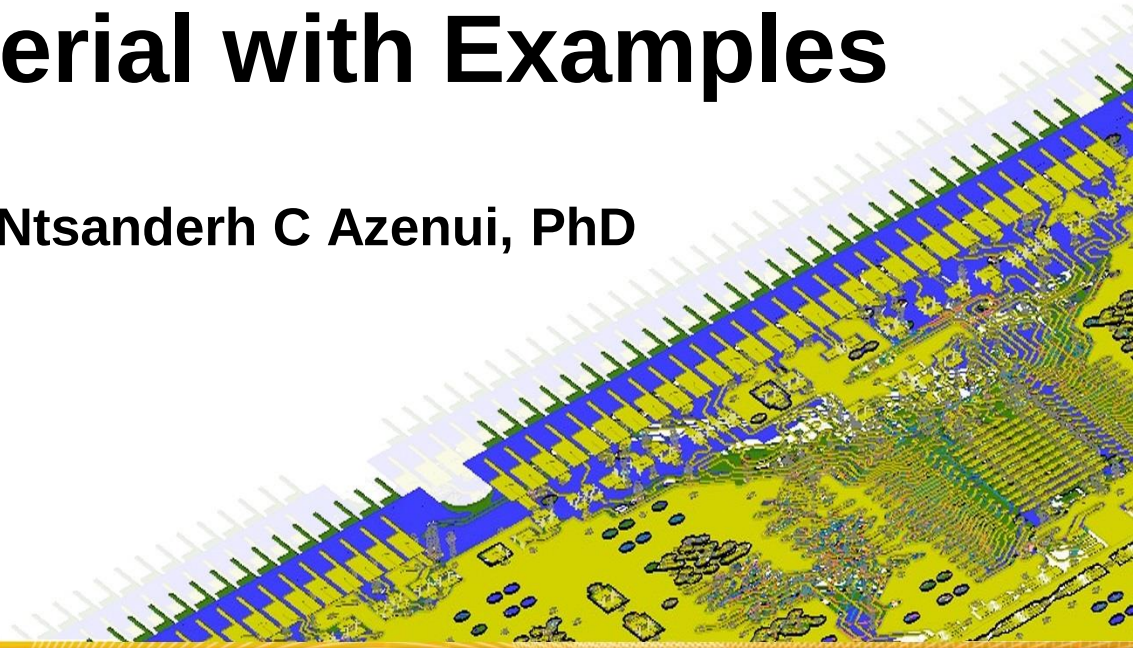
ANSYS®

SIwave-CPA

Training Material with Examples

Ntsanderh C Azenui, PhD



Legal Disclaimer

- **ANSYS product information is highly confidential and proprietary. By proceeding with ANSYS product discussions, recipients agree not to use or disclose this information for any purpose.**

- **ANSYS product information is not a binding commitment, and is subject to change in ANSYS' sole discretion. ANSYS undertakes no obligation to update product information.**

- **Purchase decisions, investments and other actions should not be taken in reliance on ANSYS product information, which may be prospective in nature, forward-looking and not guaranteed to occur.**

CPA (Chip-Package-Analysis) solver

Solver Features

- FEM quasi-static field solver. Geometry driven mesh. Uses multi-threading (HPC)
- CPA MoM (activate Q3D solver feature) uses Adaptive Meshing
- Fast, accurate **RLGC** extraction of power & signal nets for IC, Packages and PCB

Usability Features

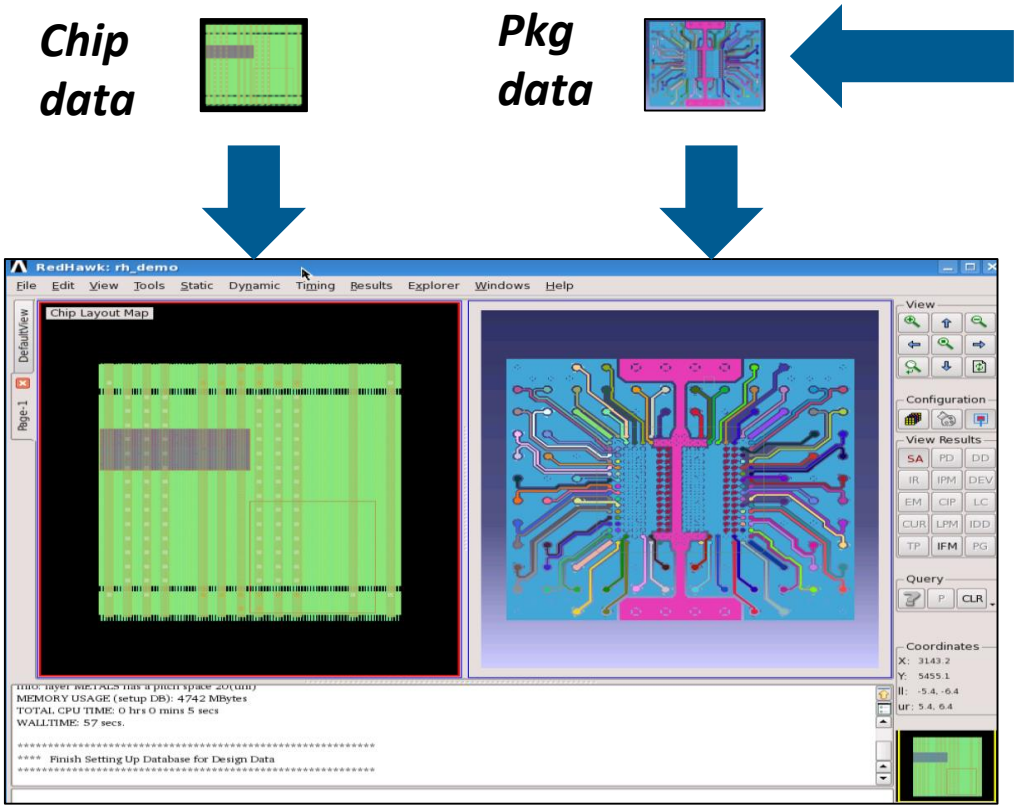
- Pin group, or Per-bump-(up to thousands)-resolution SPICE models including decoupling caps and inductors
- High Resolution graphical color maps of R and L for package probing
- IBIS RLGC Model Generation
- Scalability (handles large number of nodes, eg. 5000)
- Chip + package co-design either in SIwave or Redhawk with CPM file addition

Applications

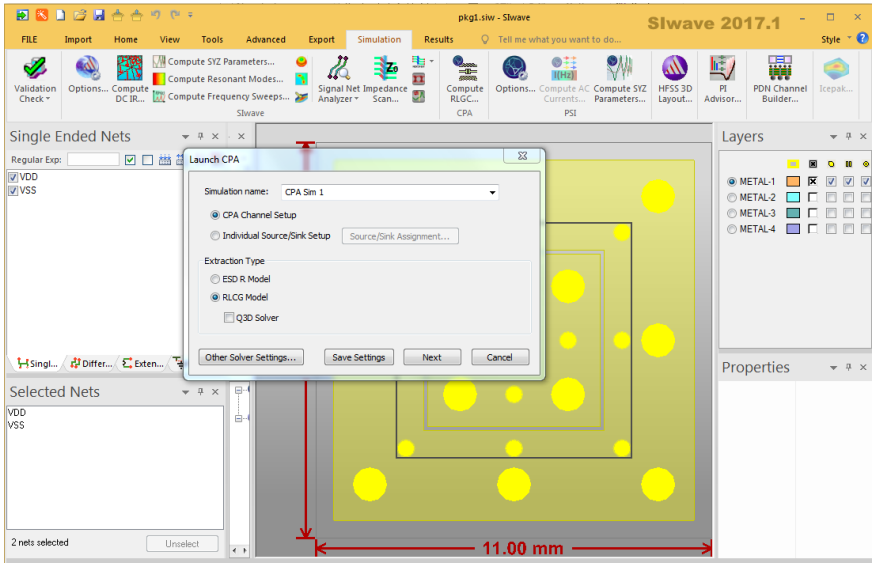
- **Package/PCB electrical engineers:**
  - **RLCG extraction of RDL, PKG and PCBs (DC RL, and frequency dependent AC RL and CG)**
  - **User selectable solver choices (FEM or Q3D-MoM solvers)**
  - **Probe the layout weakness – do design iterations – PDN system – DC to GHz's – individual bump level – fast turn around**
  - ***SI analysis – quick extraction of 100's of signals – IBIS model generation of RLCK – quick scan of signal properties***
  - ***PCB RLCG modeling including the passive RLC components***
  - ***Broadband S-parameter export from RLCG data***
- **Chip engineers:**
  - **Include the package effects into Chip simulations – cosimulation of chip+pkg – hotspots – codesign – covisualization of results**

Chip-Package Coanalysis and Codesign

RedHawk and Totem



SIwave-CPA



- CPA model generation in SIwave.
- Model exchange into RedHawk for cosimulation and covisualization of results.

SIwave-CPA Highlights

Technology

- Uses 3D FEM and 3D MoM solvers
- Similar to PSI and Q3D solvers
- Extracts RLCG netlist
- Frequency dependency
- Ground bounce preserved

Accuracy

- PDN analysis with FEM solverSelect MoM solver (Q3D) for better accuracy.
- Performance-Accuracy trade-off

System Flow and Usage

- Integrated into Ansys Chip tools
- Integrated into Ansys SIwave
- Very easy to use and detailed reports

Performance/Capacity

- Very high capacity FEM solver – full package and PCB structures – 10,000's of sources/sinks
- Fast extraction (minutes to a few hours – even for extremely large packages with over 10K bumps)
- Distributed computing (HPC)

Applications

- Silicon Interposer and RDL
- Thru Silicon Via (TSVs) structures
- Packages
- PCBs – Power Electronics
- Supports decaps, and embedded components
- PI and SI analysis
- IBIS modeling
- Wideband Spice models

R19 SIwave-CPA Highlights

Solvers

- Fast RLCG extraction at per-bump level with high granularity
- Rigorous MoM solver (Q3D) for high accuracy applications
- Distributed computing (HPC)

Models

- Broadband Spice netlist and IBIS model generation
- ESD and CPA models for ANSYS RedHawk/Totem Chip-Pkg-System cosimulations

Results

- Detailed reporting capabilities including:
  - RLCG spreadsheets
  - Pin level color maps of resistance and inductance
  - Spice netlist's compatible with all mainstream Spice simulators
  - HTML reports including the complete setup, geometry, and the results. Interactive control of results in the report for customization.

R19 SIwave-CPA Highlights

Flexible Source/Sink Setup

- Traditional CPA setup (Die, BGA and PDN components)
  - RedHawk generated PLOC import
  - Chip Power Model (CPM) import
- Individual source/sink setup, with ability to float pins

Flexible Choices

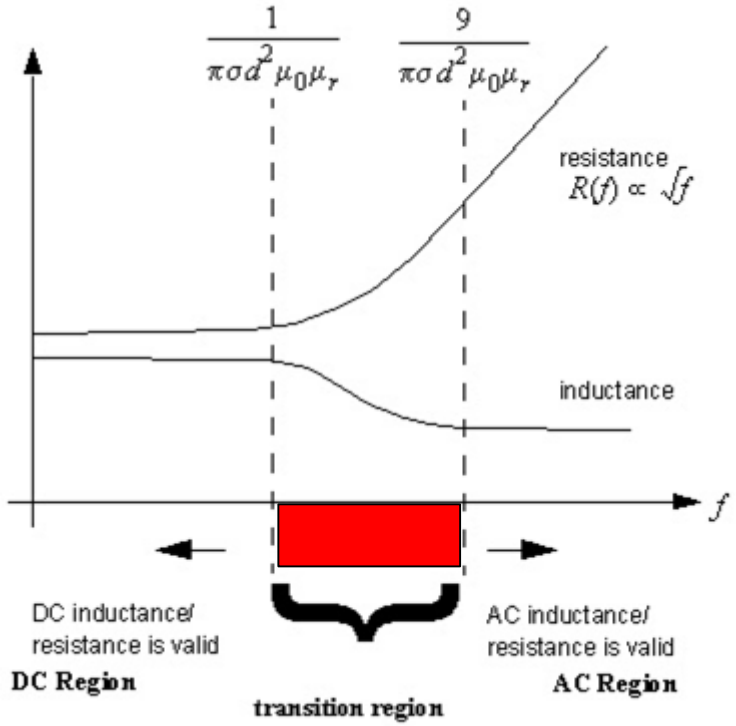
- User-defined extraction frequency (both FEM and MoM solvers)
- Independent selection of DC RL, AC RL and CG extractions for Q3D
- A new fast and robust mesher coupled with adaptive refinement
- Ground planes above and below the structures supported for Q3D

CPA-Q3D: HPC Performance

Project name	Machine number	Total Runtime (H:M:S)	Peak memory(MB)
	1	1:36:51	13080
	2	0:50:31	9716
(30 nets + 72 source ports)	4	0:44:09	8862
	8	0:23:15	8516
	1	1:06:45	9696
	2	0:30:08	8787
(77 nets + 211 source ports)	4	0:21:38	8226
	8	0:16:55	7274
	1	0:58:28	12512
	2	0:39:10	9260
(38 nets + 97 source ports)	4	0:29:07	8474
	8	0:24:55	8206
	1	1:09:40	9995
wirebond	2	0:31:06	9957
(230 nets + 230 source ports)	4	0:19:56	9708
	8	0:15:16	8487
note:			
Each machine uses 8 cores			
Peak memory is for master node			

Some Key Technical Details of CPA solver

- Quasi-static approx. is a simplification of Maxwell's equation for electrically small structures. Rule of thumb: "**structure size < lambda/10**" at maximum freq. of interest
- Depending on the options selected for "**Select Parameters to Compute**," CPA
- Solves (CG & RL) at DC
- Solves (CG & RL) at AC using the entry for **"G+RL frequency"** as the solution frequency Surface current (skin depth) is well developed, and **quasi-static approx**. (structure size<lambda/10) holds
- Blends AC and DC solution in the transition region



d is conductor thickness

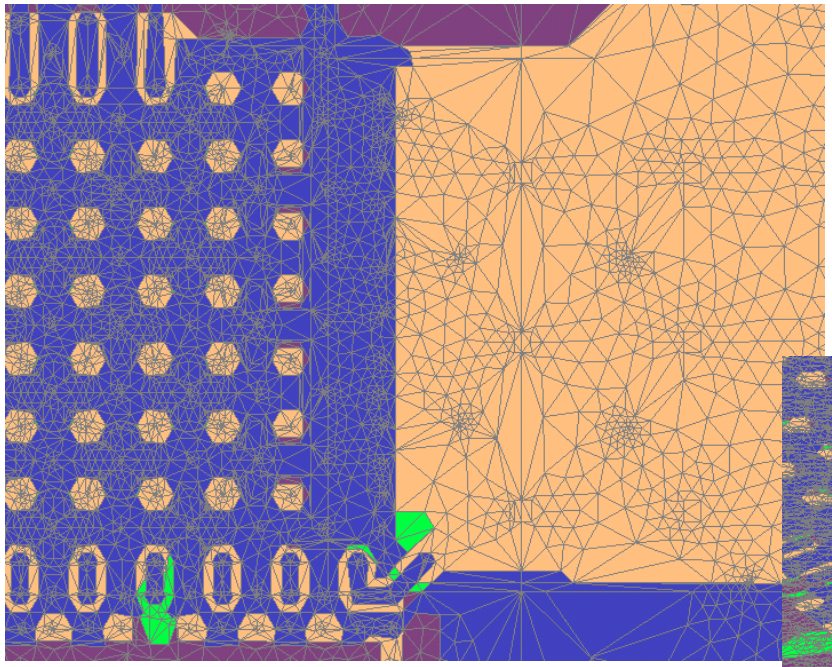
- The Quasistatic approx. allows to solve Poisson equations for the electric and magnetic potential functions **Phi** and **A**
- V = grad (Φ); grad^2(Φ)=ρ; grad^2**(A)+**k^2***A=J**
- where V and **J** are the excitations
- The charge, Q is then derived from **Phi** and find CG from (G+jωC)V=jωQ
- R and L derive from the surface current distribution, the surface impedance Z = sqrt(2j)/(σδ), and **A**

  Z = R+jωL

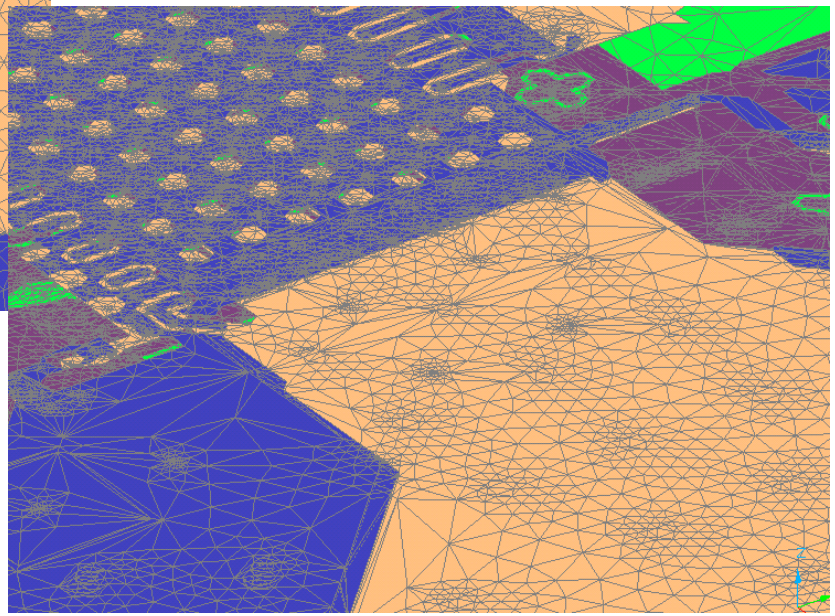
CPA – FEM Solver

- FEM Solver is based on 3D modeling – similar to SIwave-PSI solver
- Geometrical objects such as microstrip/striplines, vias, pads, etc. are all modeled as volumetric metallic objects with finite conductivity
- Volumetric elements (Prisms) are placed inside the via barrels, traces and shapes
- Dielectric objects are modeled as such using 3D elements with lossy material
- FEM solution assumes that RL and CG are decoupled in the quasi-static limit and can be extracted separately.
- This is similar to MoM approach of Q3D solution.

FEM Meshing: Fast Conformal Meshing



- Conformal composite mesh elements
- Identification of domains and key geometry areas



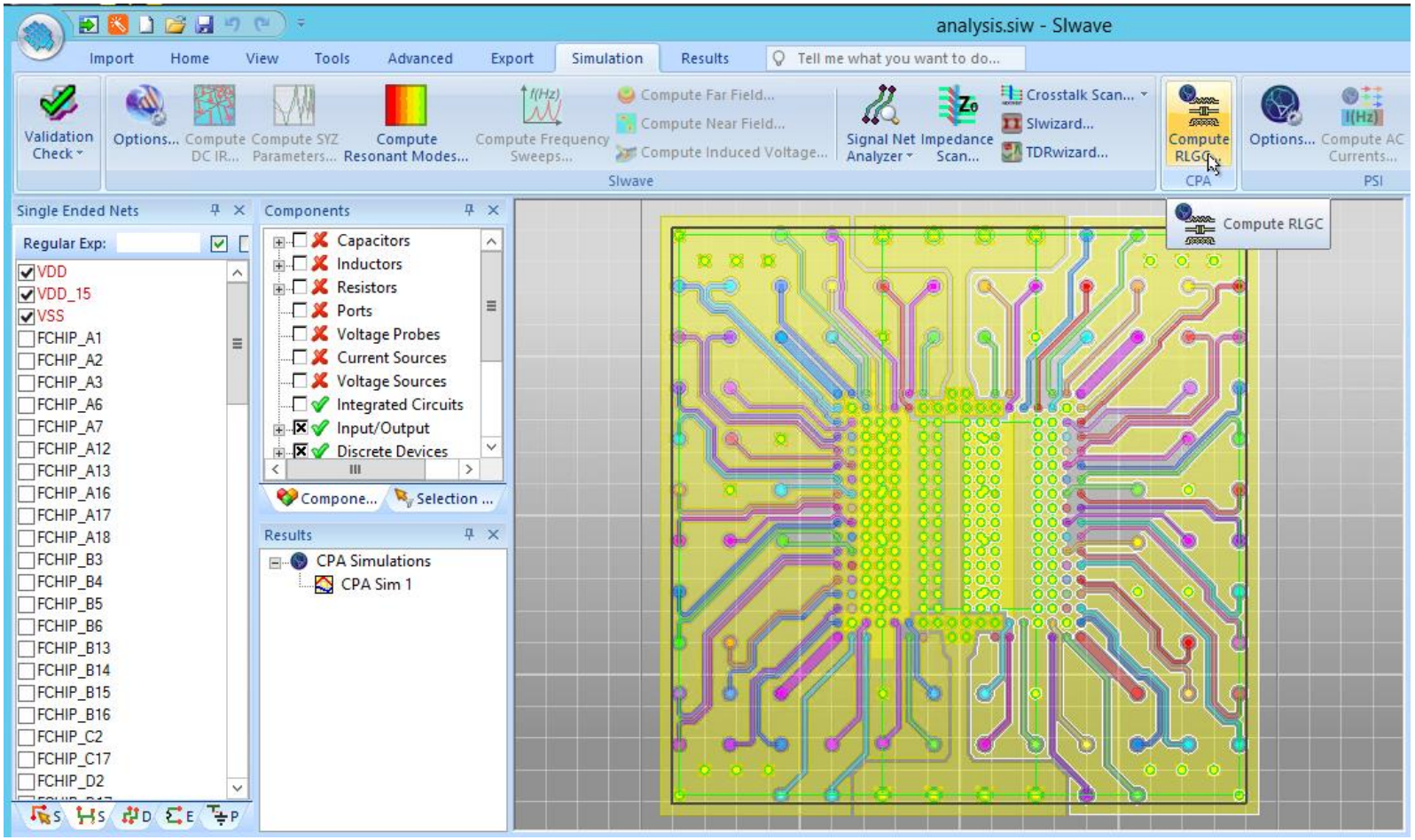
Mesh technology is critical for high capacity simulations. Proper use of higher-order elements helps in controlling number of unknowns.

FEM Solver: Key to a Fast RLCG Extraction

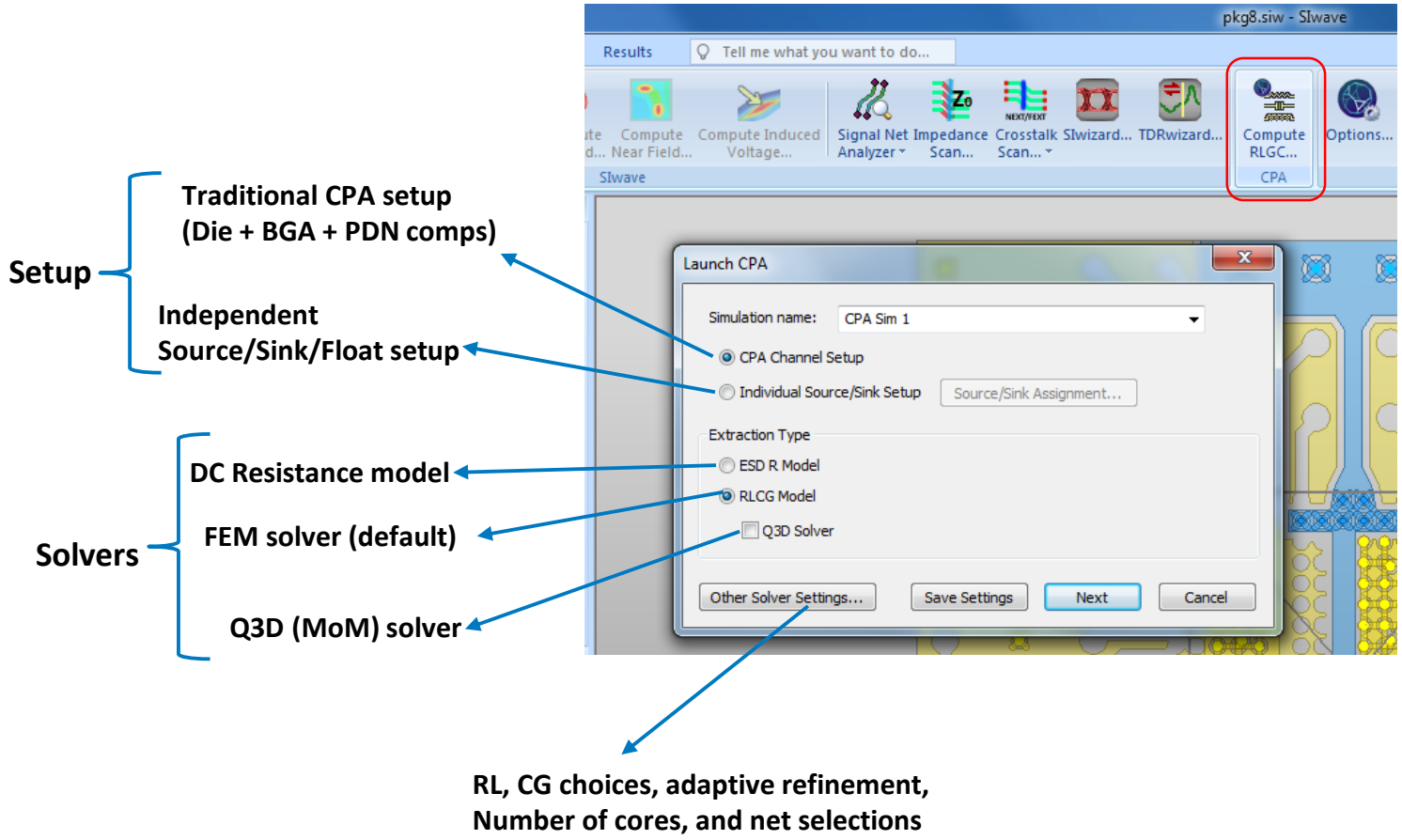
- Sparse nature of FEM matrices
- Mature technology of the fast Sparse matrix solver
- Direct matrix factorization – Only once
- Forward-Backward substitution for multiple right-hand-sides (1000's of RL branches) – very fast extraction of per-pin RL
- Highly multi-threaded solver

General Setup and Usage

SIwave-CPA



Setup



Note: Q3D solver extracts the whole geometry without any partitioning of structure.

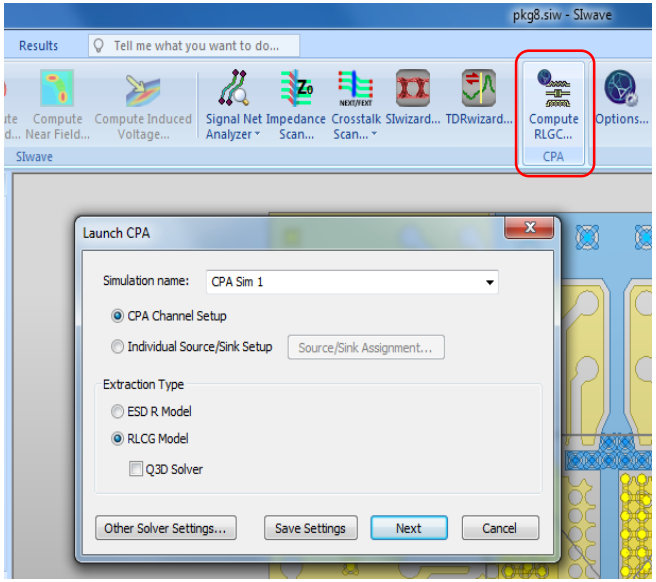
Solver Selection Recommendation

FEM Solver

- No limit on number of sources and sinks
- Packages and PCBs with well defined ground planes
- Large scale PDN structures
- RDL, Silicon Interposers, TSVs
- No limit on number of Signal lines

MoM Q3D Solver

- Limited number of sources and sinks
- Leadframe designs
- Wirebond packages
- Smaller flip-chip designs
- SI analysis with “fewer” lines
- Can handle larger designs – based on memory/run time requirements



Note: We use FEM solver by default, unless Q3D solver is selected.

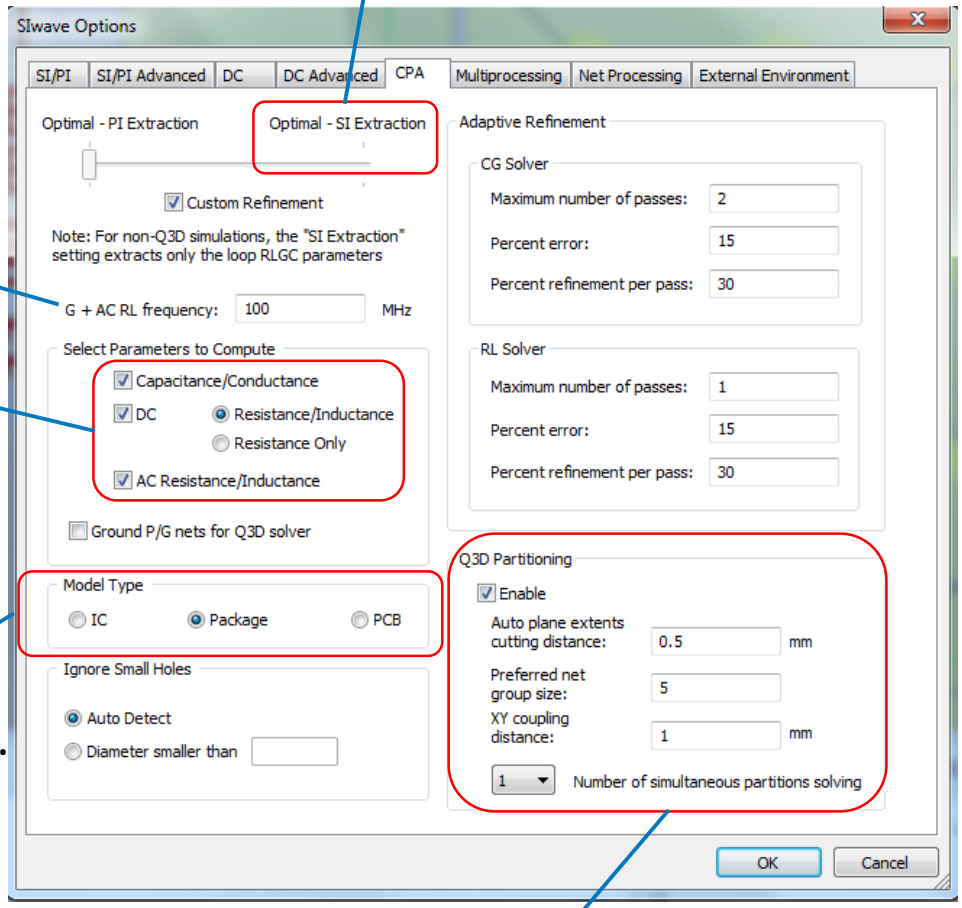
Note: Do not compare <u>partial</u> RLCG data between FEM and MoM solvers. They use different global reference. We can only compare Loop-RLCG results across solvers.

CPA Options

Use FEM solver with this setting for a fast and accurate extraction of 100's of signal nets.

FEM solver: Must be before 1st resonance. Typically, 100MHz for packages, and in KHz for PCBs.
Q3D: High enough for skin-effect to manifest.

Select both DC RL and AC RL together

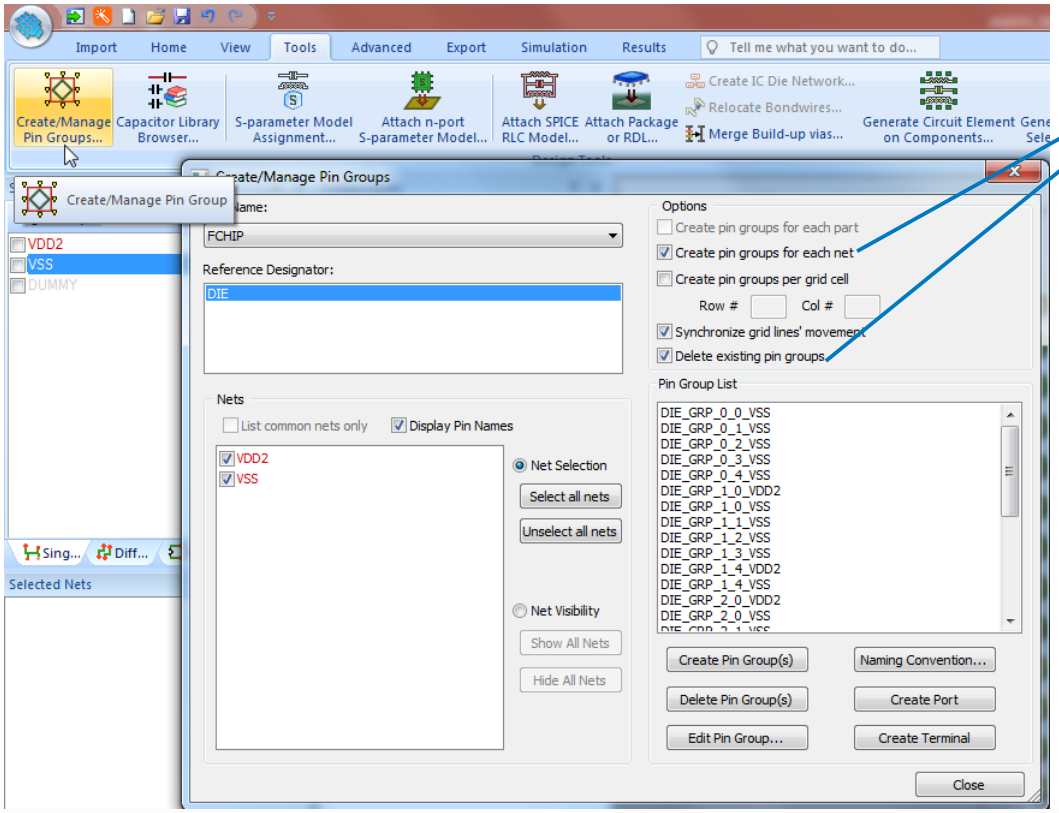


IC: for RDL, interposer, etc.
Package: for wirebond, flip-chip, etc.
PCB: use for PCBs
PKG+PCB: Select Pacakage type

- **Refer to HELP.**
- **Recommended only for SI extraction with large number of signal nets.**
- **Recommend to select Ground P/G nets for Q3D solver option.**

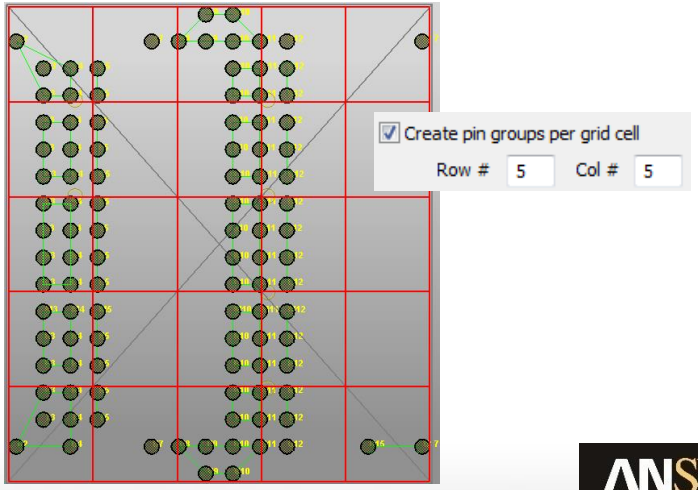
Importance of Pin Groups

- **Extraction is controlled by user-defined pin groups defined in the project.**
- **If RedHawk PLOC (or CPM) file is imported into SIwave, it also creates pin groups and these are subsequently used for extraction.**
- **Sources and Sinks can be defined on the pin groups.**

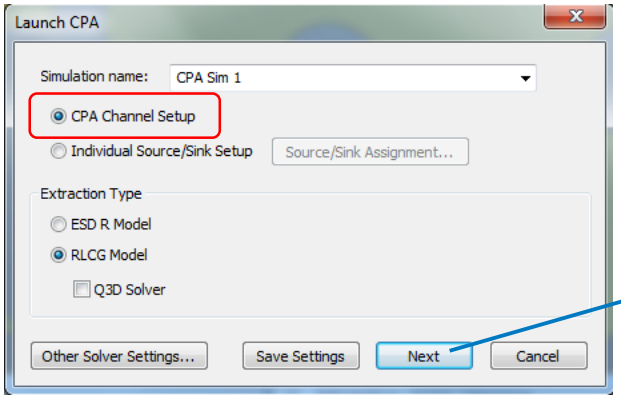


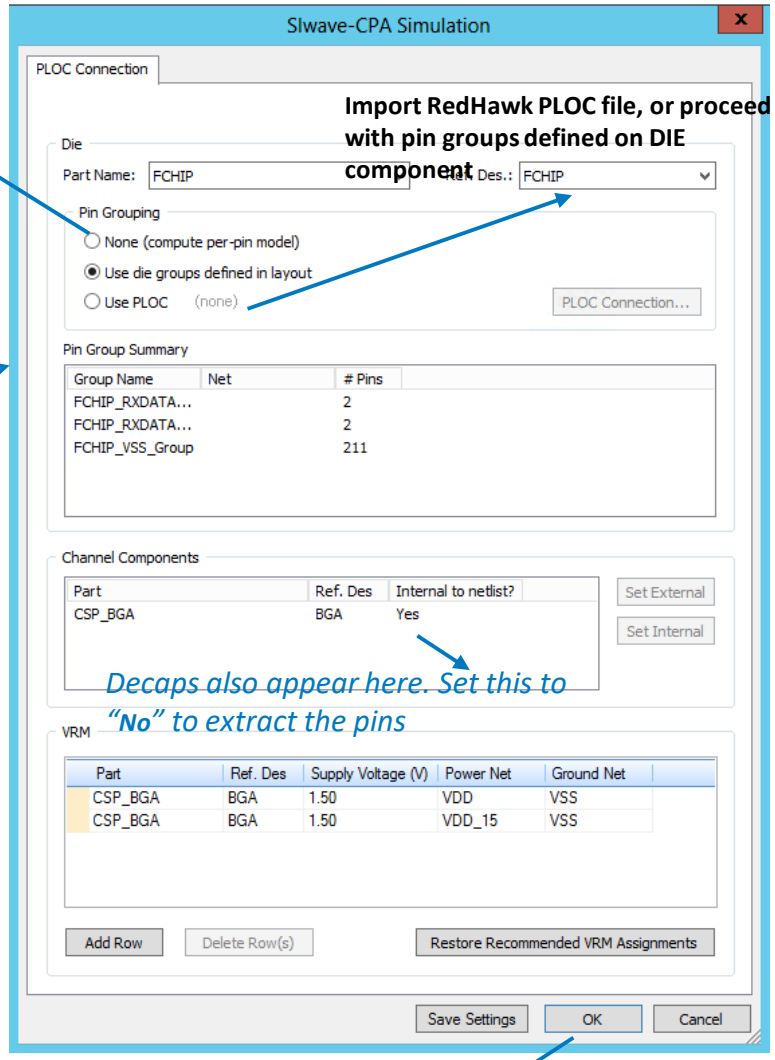
Make sure to check these boxes while creating pin groups. Otherwise, pin groups would be created across nets, and there could be duplicates – Not supported for extraction.

Pin groups can also be created on rectangular cells for the selected reference designator.



CPA Channel Setup





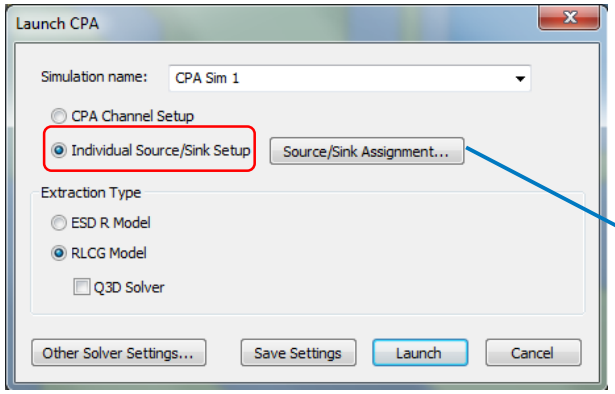
Majority of the structures have two or more components to be extracted. Without loss of generality, let us call them DIE, VRM and PDN components.

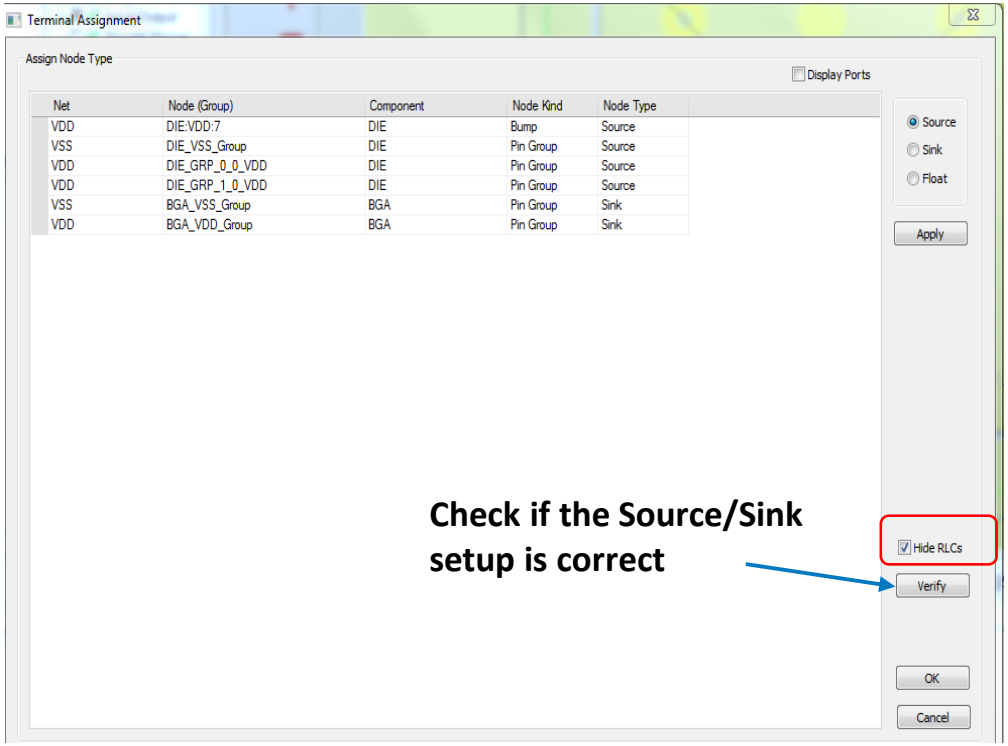
- **Select a component as the DIE component – all of its pins become sources.**
- **Select a component as the VRM component – all of its pins become sinks.**
- **Any other components (second die, decaps, etc) are left as Channel components. Set their "Internal to netlist" flag to NO, if they also need to be extracted.**
- **Specify a supply voltage (leave as 1.5V, if not known). It has no impact on RLCK parasitics, and is only used by Chip level simulations.**

Click OK to proceed with extraction

CPA Channel Setup must be used if the model is going to be used in RedHawk for system level simulations.

Individual Source/Sink Setup



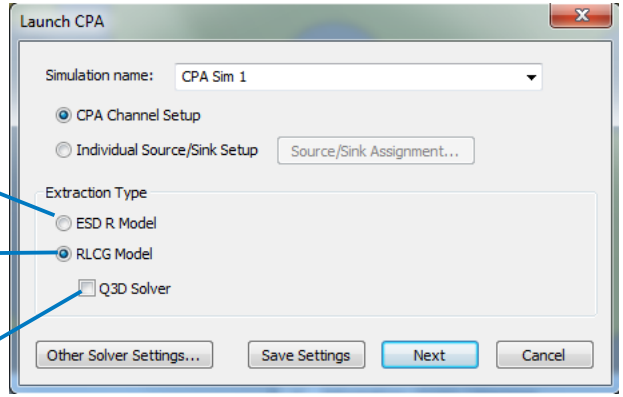


- Provides more flexible setup when needed.
- Pin groups and ungrouped pins appear in the table.
- Individual pins (groups) can be floated.
- Select multiple rows and set them as source, sink or float types.
- Note that each net can only have one sink.
- A pin group can only contain pins of same net.
- RedHawk PLOC hook-up and encrypted netlist generation not supported.
- RLCG extraction at the user-defined sources and sinks is performed.

Check if the Source/Sink setup is correct

Extraction Type (Solver choice)

Pure DC resistance extraction with the Spice netlist customized for Chip ESD applications

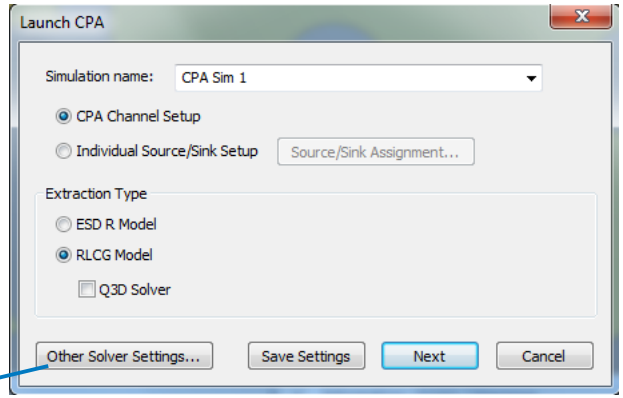


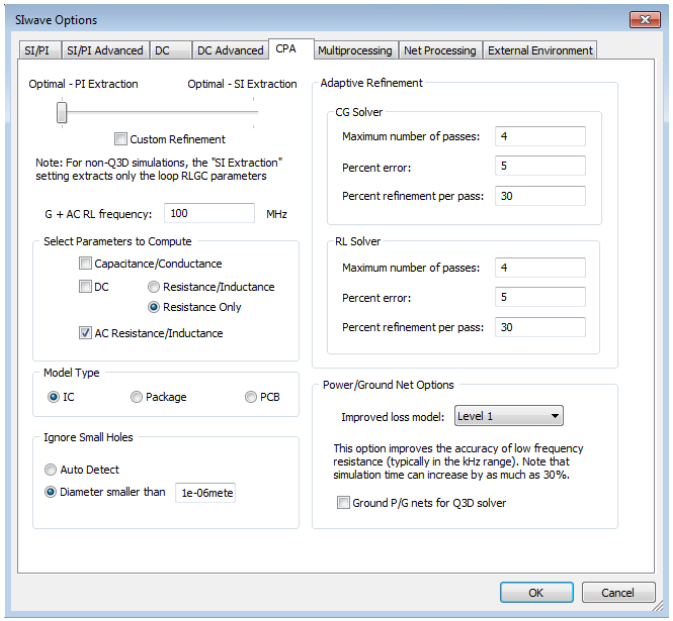
- **Uses FEM solver.**
- **High capacity and fast turn-around time.**
- **Recommended for large PDN structures and (or) having several hundreds of source terminals.**
- **Recommended for IBIS modeling**

- **Uses Q3D MoM solver with adaptive meshing.**
- **Recommended for high accuracy applications.**
- **Ideal for leadframes, small scale packages, etc.**

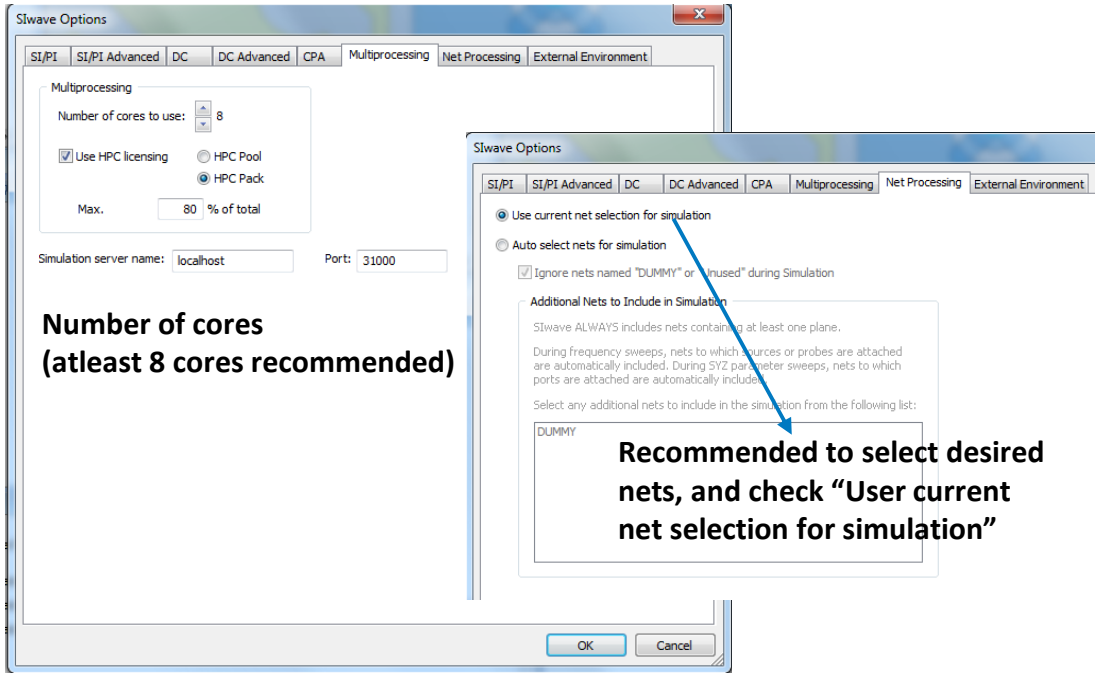
Note: ESD model always ungroups the pins on the BGA component, and extracts resistance for each and every pin. This is needed for chip-level ESD path tracing.

Other Solver Settings





Controls extraction frequency, DC/AC RL and CG setup

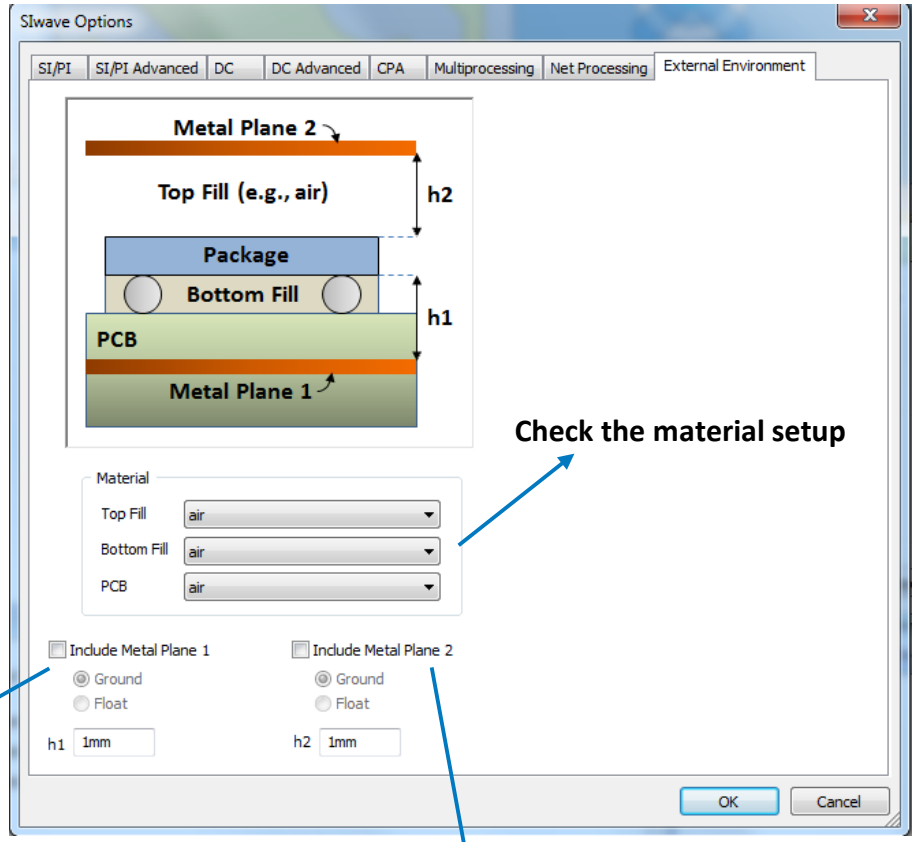


Number of cores (atleast 8 cores recommended)

Recommended to select desired nets, and check "User current net selection for simulation"

Other Solver Settings – External Environment

***External Metal planes*:**
Applicable only for Q3D MoM Solver

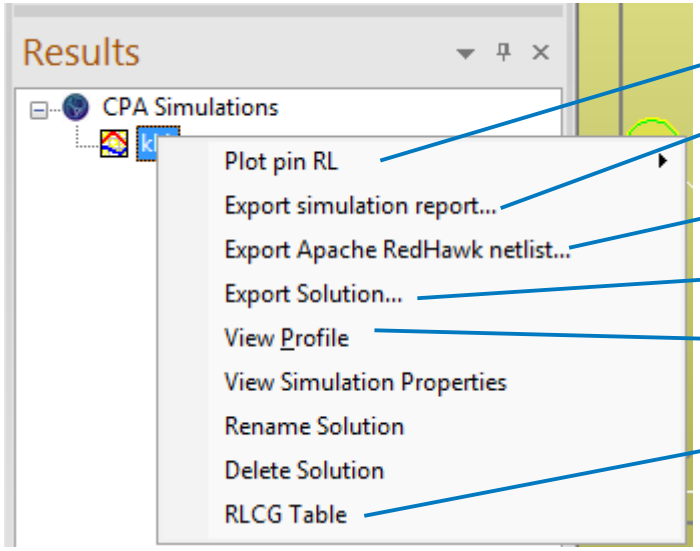


Check the material setup

- **Check the box to add a metal plane (Ground or Float) under the geometry at h1 distance.**
- **Note that "h1" is measured from the bottom of the layer stackup, not counting solder balls if present.**

- **Check the box to add a metal plane (Ground or Float) above the geometry at h2 distance.**
- **Note that "h2" is measured from the top of the layer stackup, not counting solder bumps if present.**

Description of Extraction Results



View colormap of RL data

HTML report generation

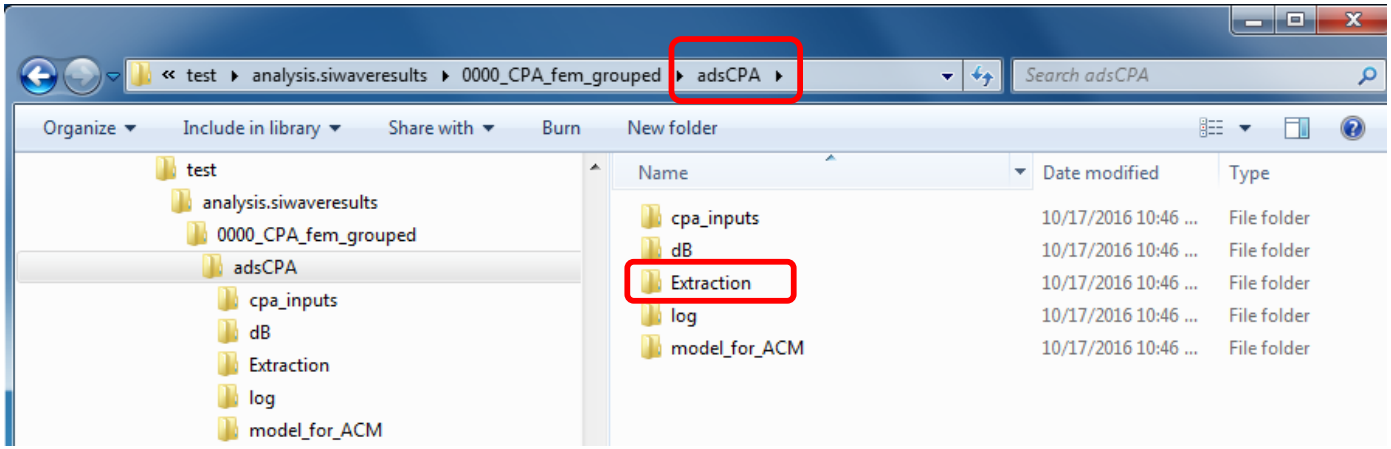
Export RedHawk adsCPA folder

Export IBIS, Spice, S-para, etc

View the log file

View results table and export to text file

Results Folder Structure



Contents of *adsCPA/Extraction* folder

AC RLCG matrices

DC RL matrices

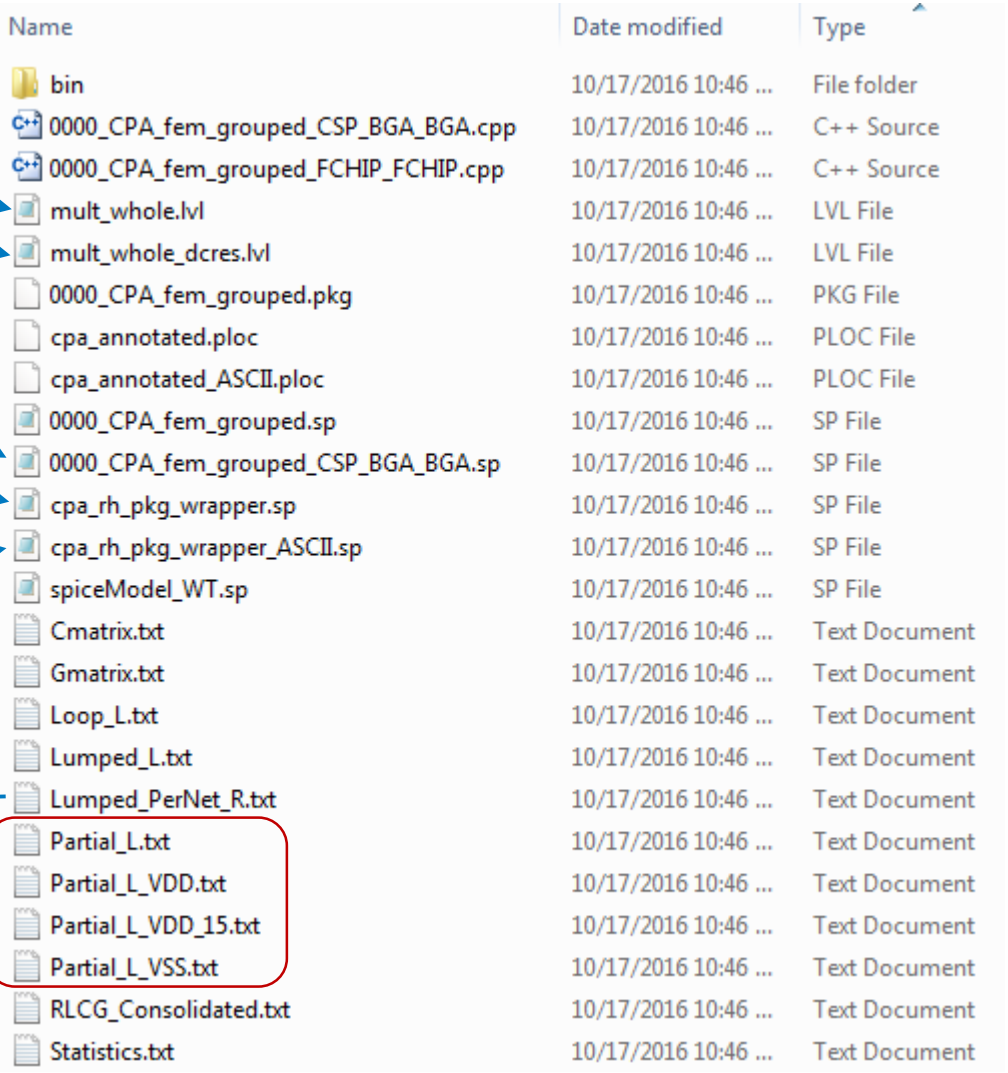
Empty BGA Spice deck (edit to add PCB models)

Encrypted wrapper for RedHawk/Totem

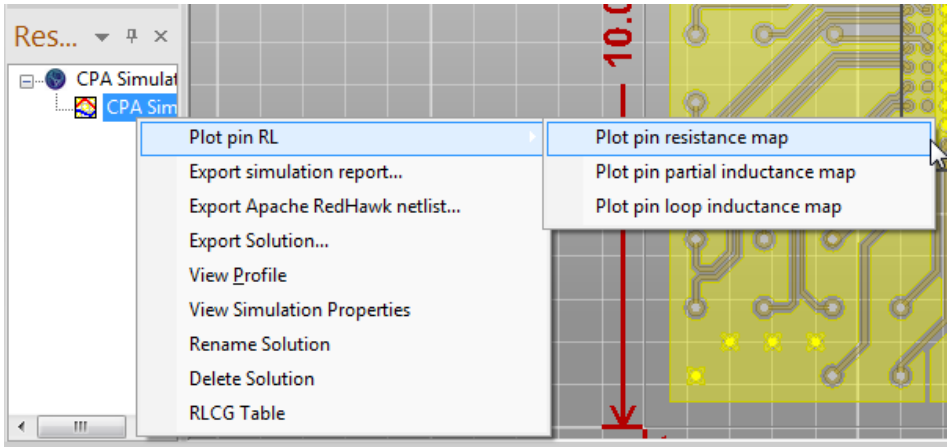
Top-level netlist for CPA model

For each net, we group all the DIE and VRM pins – compute the lumped resistance for each net (from die to VRM).

This is the partial L of each pin from DIE to VRM.

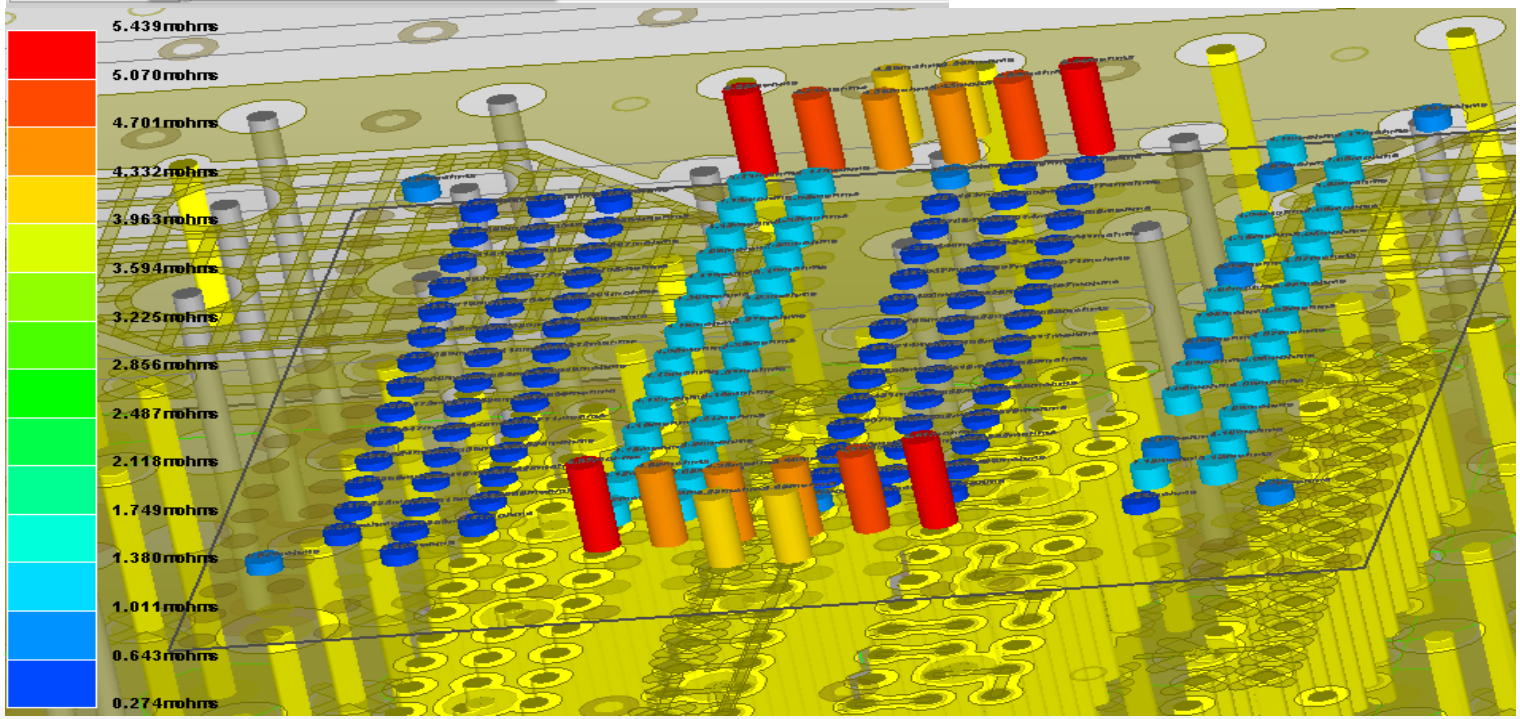


Description of Extraction Results: Pin Resistance Map

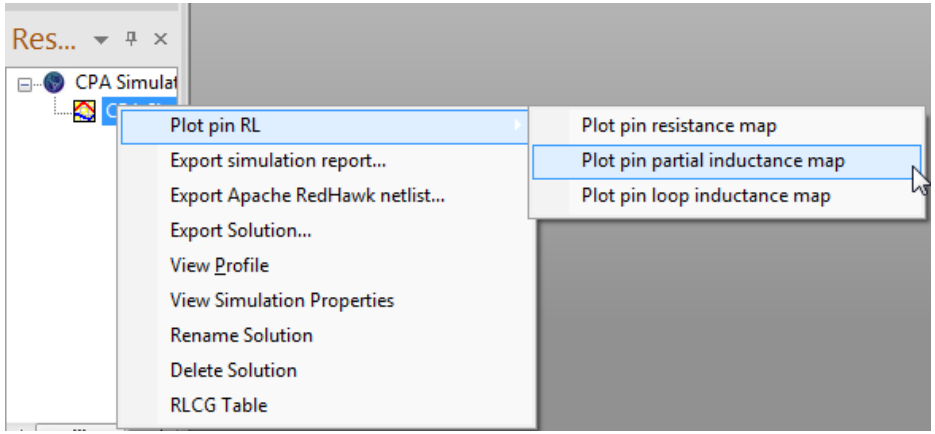


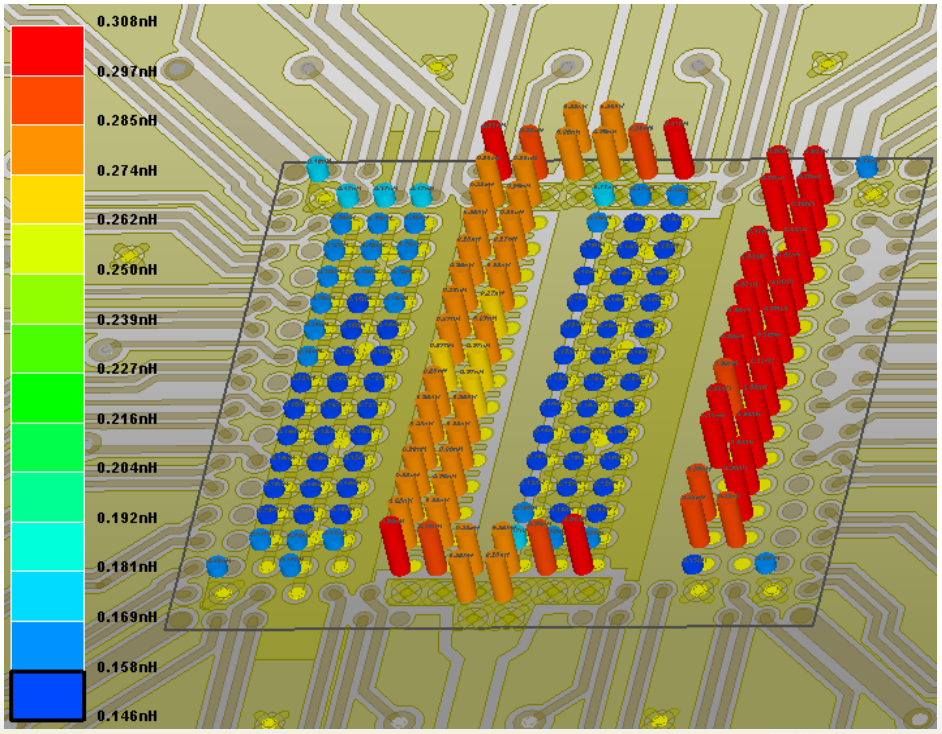
For each die pin, we compute the effective resistance to the corresponding VRM pin group of its net.

Rest of the extracted pins on the die, vrm, and pdn components are open-circuited.



Description of Extraction Results: Pin Inductance Map





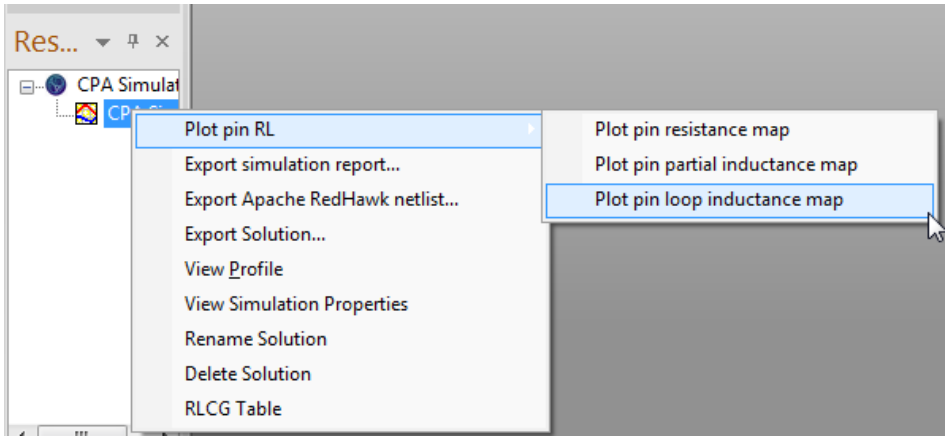
For each die pin, we compute the effective inductance to the corresponding VRM pin group of its net. This is the partial branch inductance.

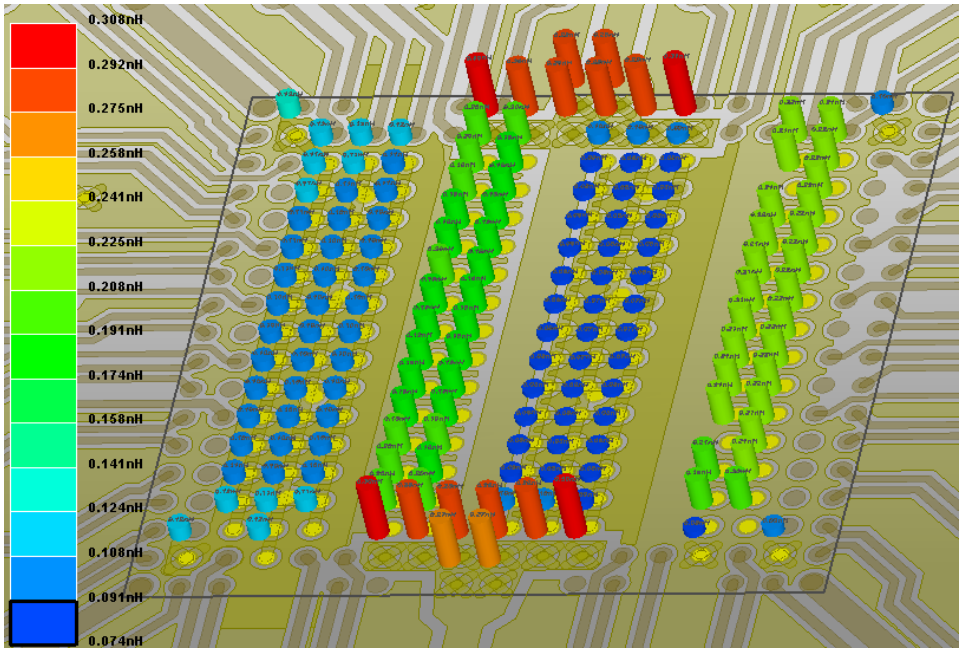
Rest of the extracted pins on the die, vrm, and pdn components are open-circuited.

While the partial inductance per-pin is a useful feature, it is not a direct indicator of how well that pin behaves in the presence of chip.

That requires the computation of Loop inductance – as each pin can take the surrounding pins as return paths.

Description of Extraction Results: Loop Inductance Map





Loop inductance is a post-processed result derived from the partial inductance matrix. (Lloop = L11 – 2*L12 + L22)

Partial inductance matrix is what is used in the Spice netlist exported for RedHawk usage.

Loop inductance is presented to only aid user in troubleshooting the package design.

For each DIE power pin, we use all of the DIE ground pins as return paths and compute the Loop-L for the power pin.

Similarly, for each ground pin, we use all the DIE power pins as return paths.

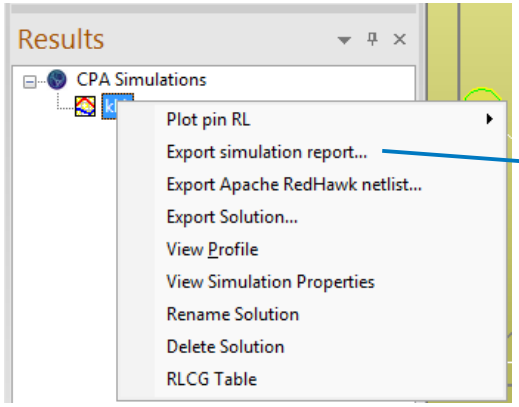
Changes in Loop-L from one pin to another can be used to located poorly routed pins.

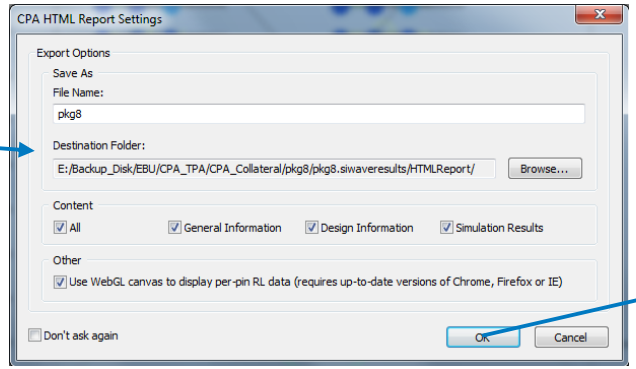
Loop Inductance Map (contd …)

VDD and VDD_15 pins use VSS as return path

VSS pins use both VDD and VDD_15 as return paths

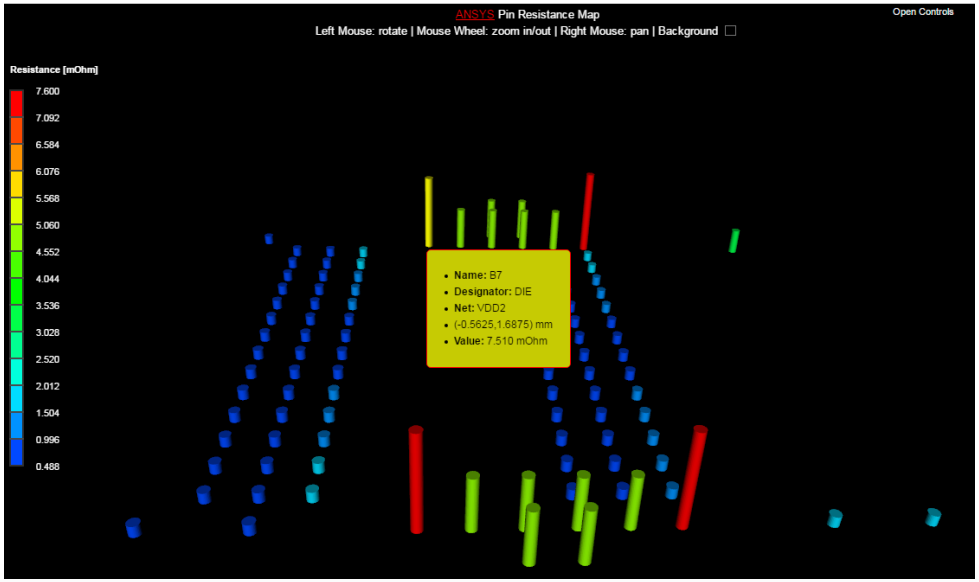
Description of Extraction Results





HTML Report

Interactive 3D Display of RL data in the HTML Report



SIwave CPA Simulation Report

Table of Contents

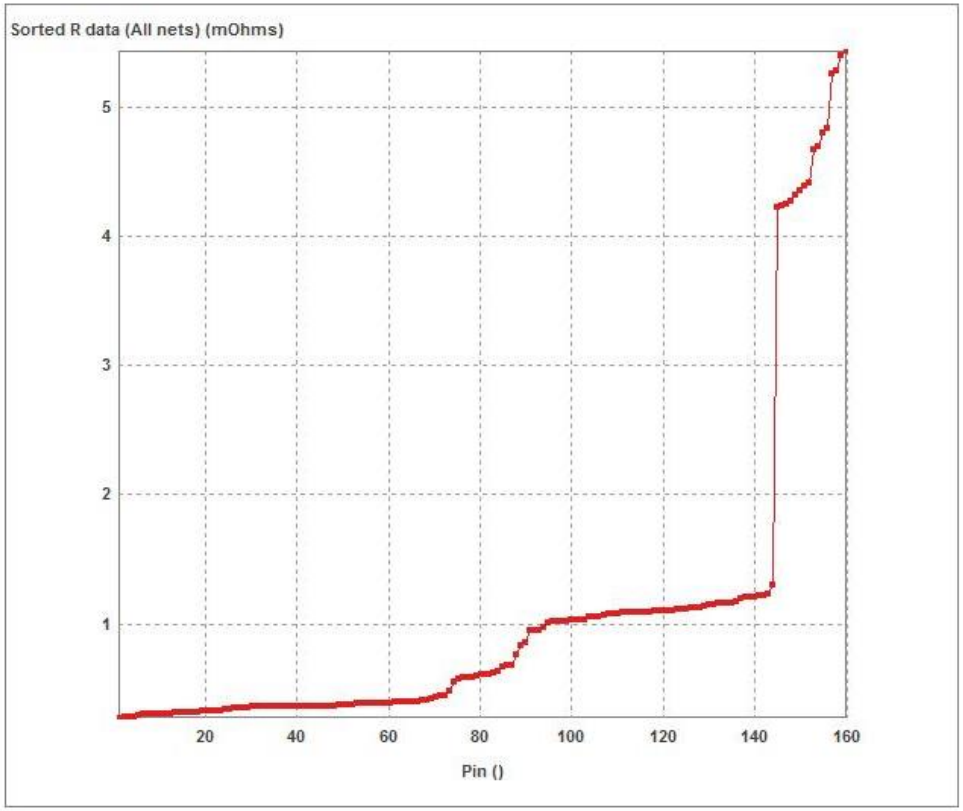
A comprehensive report of the layout, setup and the analysis of simulation results is presented in the HTML form.

Colormaps in the report are interactive in nature and can be modified within the report.

Histograms and 2D plots of the results are also presented.

HTML Report Description

Sorted R data (All nets)



For each die pin the effective resistance is plotted.

The resistance is sorted from low to high so that identifying how pins are outliers would be easy.

Similarly, the sorted (low to high) data for inductance is also available.

cpa_control.xml

User can edit this file to do certain things not yet available in the GUI.
Keep this file at the location of the .siw project file and run simulation.

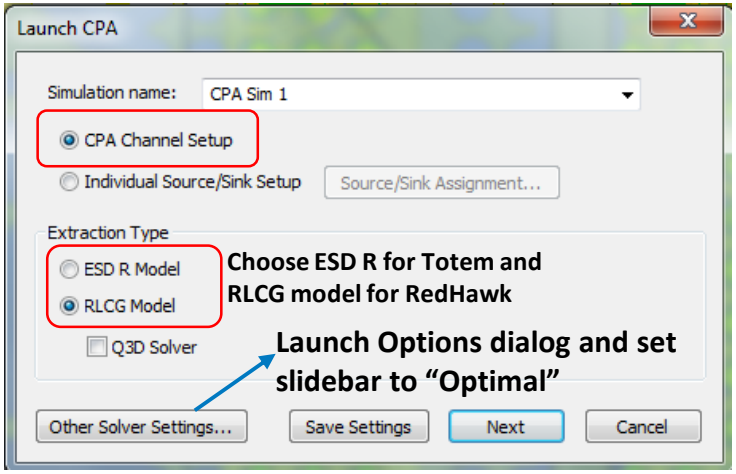
cpa_control.xml

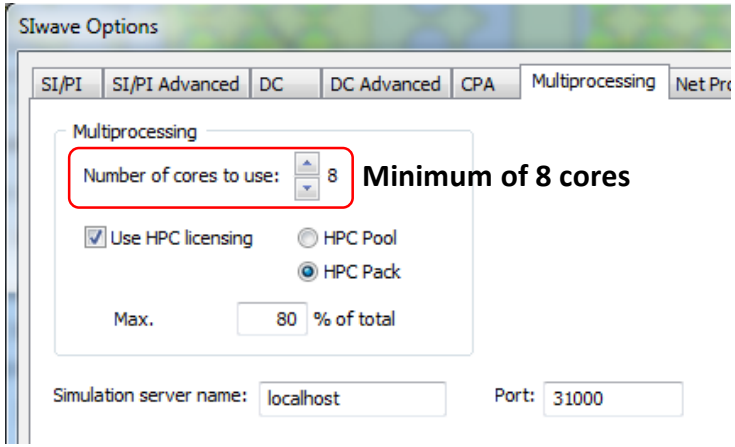
```
<?xml version="1.0" encoding="utf-8"?>

<!-- This file need to be placed in the same folder as SIwave project file (***.siw) -->
<!-- Individual sections can be disabled by setting Enable=No -->

<CPA_Control_Specs>

<!-- If enable, the annotated ploc file would use this chip layer name -->
  <Chip_Layer_Name Enable="yes" Name="ic_m1_layer">

<!-- All units in mm and are in package DIE coordinates -->
<!-- Only the die pins (having PLOC connections) falling within this polygon region gets extracted -->
  <Partial_DIE_Region Enable="no">
    <Point x="-5.0" y="5.36"/>
    <Point x="-5.0" y="0.37"/>
    <Point x="5.5" y="0.37"/>
    <Point x="5.5" y="5.36"/>
  </Partial_DIE_Region>

<!-- Voltage values are in volts -->
<!-- The unconnected PLOC pins corresponding to these Chip nets are terminated with voltage supplies -->
  <Open_PLOCpins_VoltageSupply Enable="no">
    <Net Name="NewNet1" Voltage="1.2847"/>
    <Net Name="NewNet2" Voltage="2.384"/>
  </Open_PLOCpins_VoltageSupply>

</CPA_Control_Specs>
```

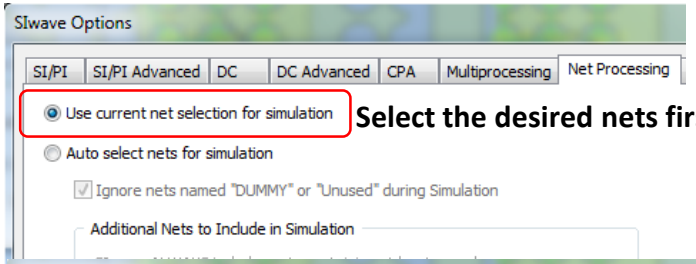
Application Specific Examples

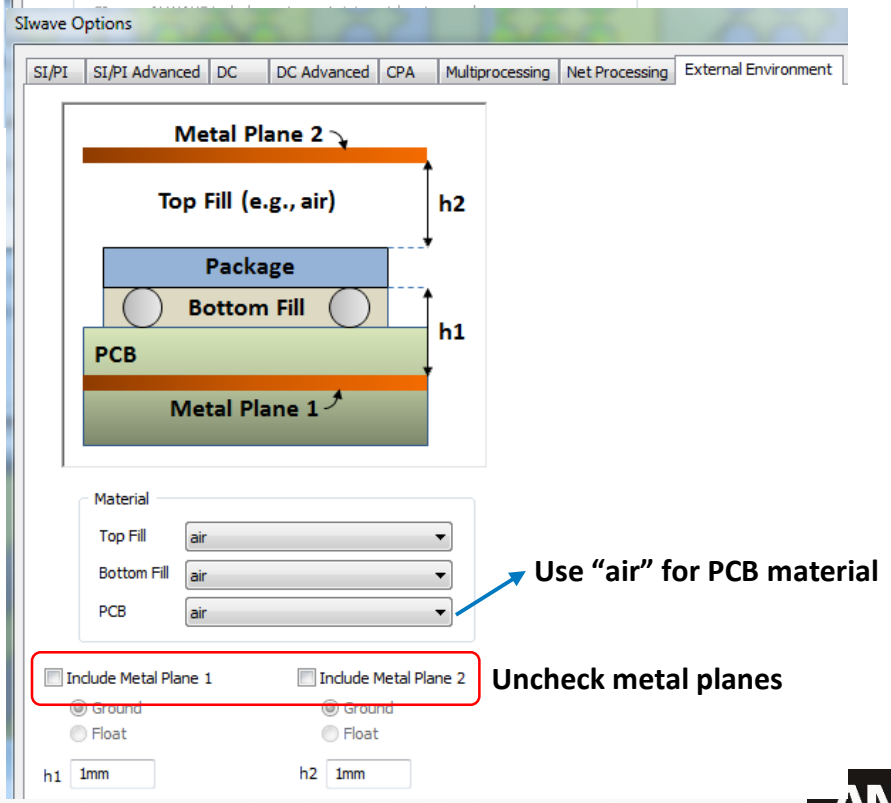
Model Generation for ANSYS RedHawk and Totem

Recommended Setup

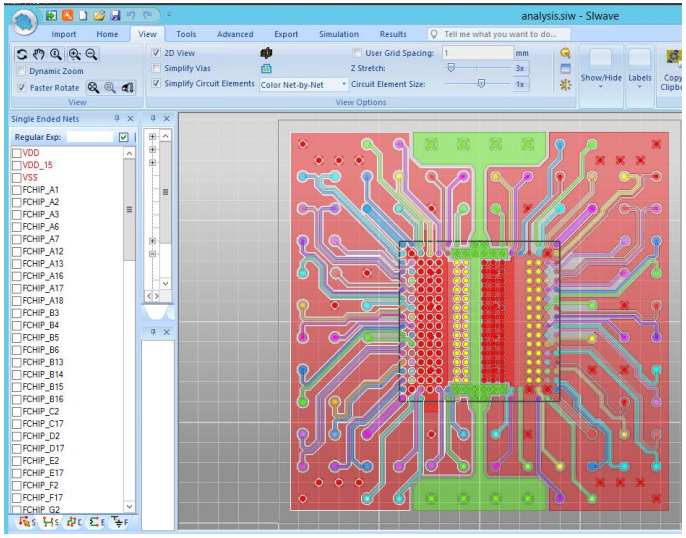






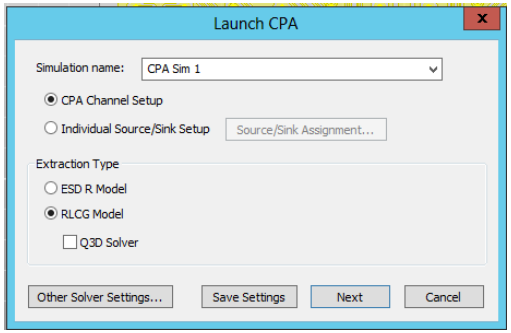


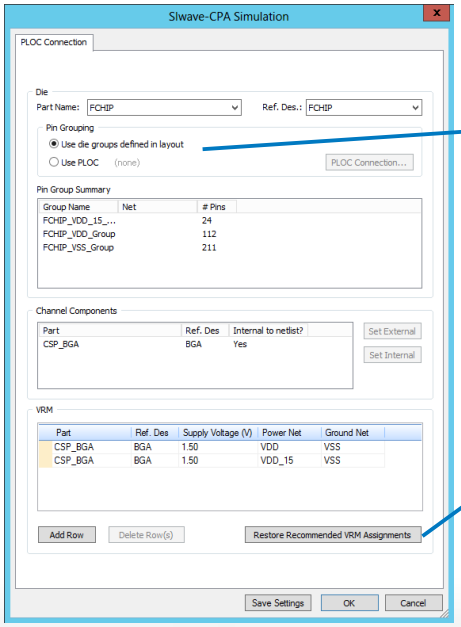
Model Generation for ANSYS RedHawk



PDN System setup for RedHawk CPA model

- Select VDD, VDD_15 and VSS nets.
- Create pin groups on DIE and BGA components. Pin groups on DIE component can be skipped, if a PLOC file is available.

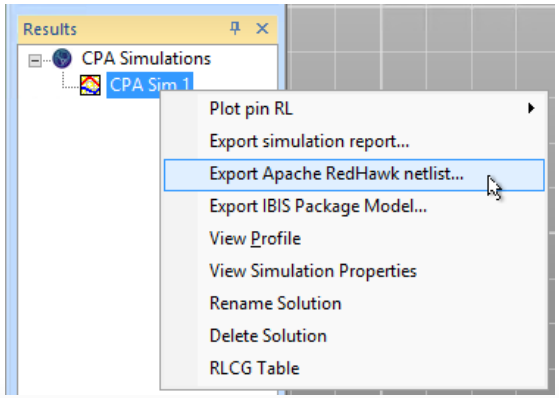




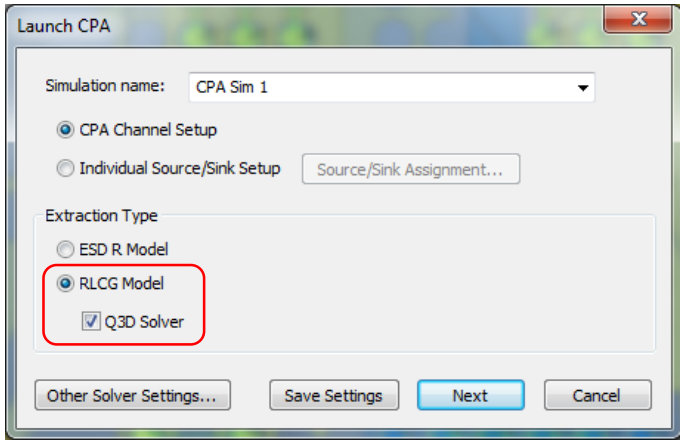
Import PLOC (if available), or use existing pin groups.

Restore recommended settings, and then setup proper supply voltages.

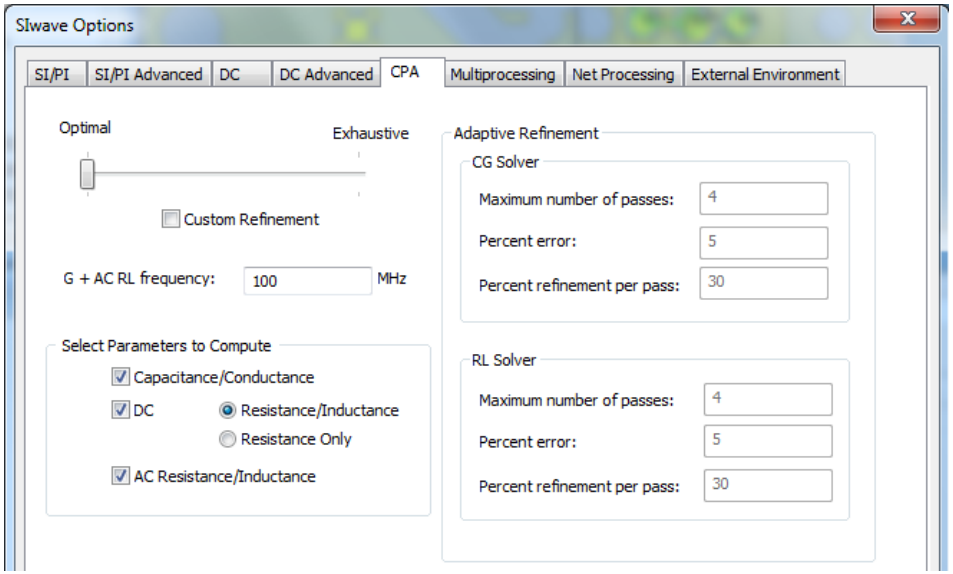
- Proceed with extraction.
- Export RedHawk netlist from the results.



General RLCG Extraction



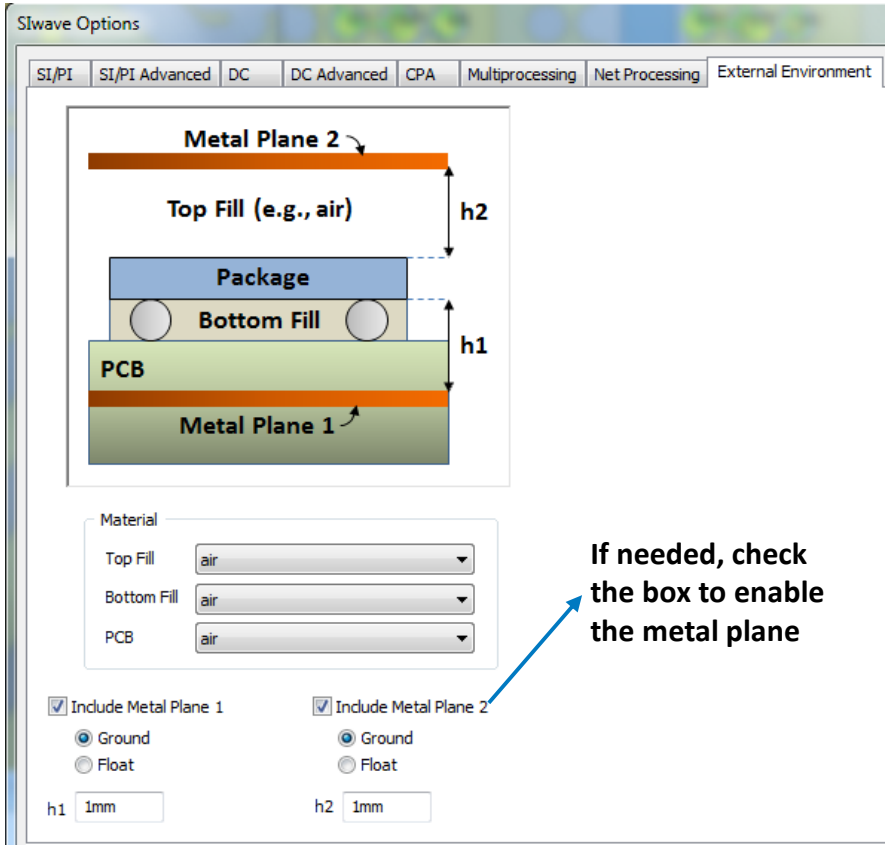
- Choose appropriate setup (Channel setup or Individual Src/Snk setup)
- Selecting RLCG Model enables high capacity FEM solver: ideal for PDN analysis of large structures and those requiring 100's to 1000's of terminals
- Choose Q3D solver for high accuracy application needs, which also allows independent extractions such as, DC RL only, AC RL only or just the CG extraction (or some combinations of those)



- Extraction frequency and adaptive refinement parameters can be custom set, or left at default.
- Recommendations for Multiprocessing, Net Processing and External Environment are same as before (atleast 8 cores, use current net selection, etc.)

External Metal Planes

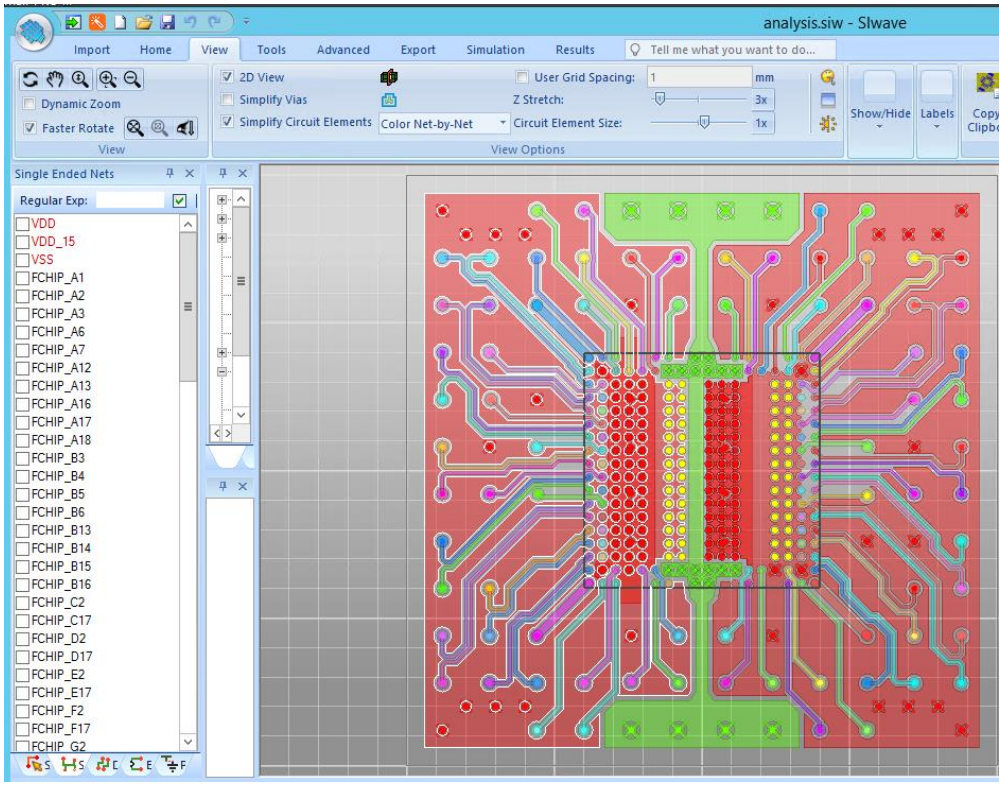
Some applications may require the presence of top and bottom metal planes.



If needed, check the box to enable the metal plane

- **Each of the metal planes can be grounded (shorted – at internally generated terminals for inductance calculations).**
- **They can be floated (or open-circuited).**

Package IBIS Model Generation



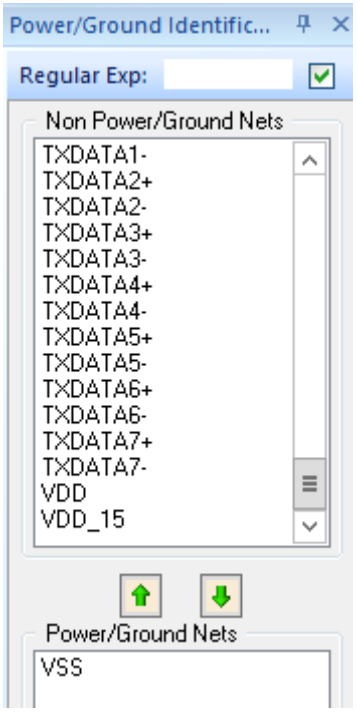
3 Power/Ground nets
All Signals on the package

Set dielectric fill to EDB_FR-4

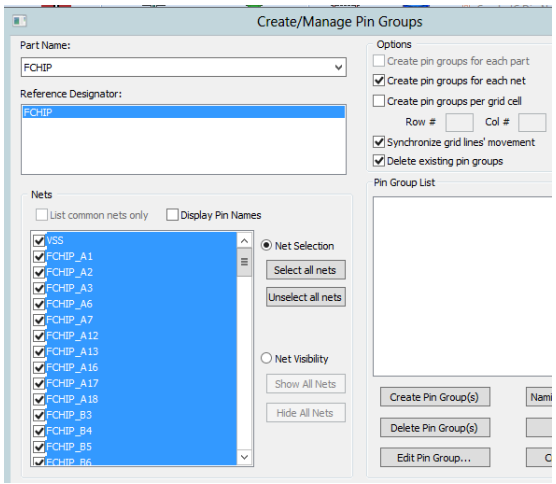
Color	Name	Type	Thickness (microns)	Material	Conductivity (S/m)	Dielectric Fill	Dielectric constant
	TOP	METAL	30.48	EDB_COPPER	5.959E+07	EDB_AIR	1
	UNNAMED_002	DIELECTRIC	203.2	EDB_FR-4	0		4.5
	VDD_C1	METAL	30.48	EDB_COPPER	5.959E+07	EDB_FR-4	4.5
	UNNAMED_004	DIELECTRIC	203.2	EDB_FR-4	0		4.5
	VSS_C1	METAL	30.48	EDB_COPPER	5.959E+07	EDB_FR-4	4.5
	UNNAMED_006	DIELECTRIC	203.2	EDB_FR-4	0		4.5
	BOTTOM	METAL	30.48	EDB_COPPER	5.959E+07	EDB_AIR	1

Package IBIS Model Generation

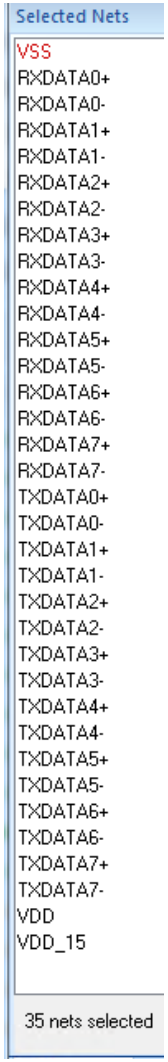
Step-1



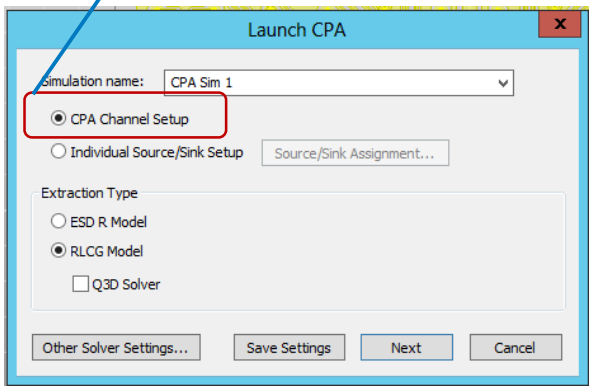
Step-2

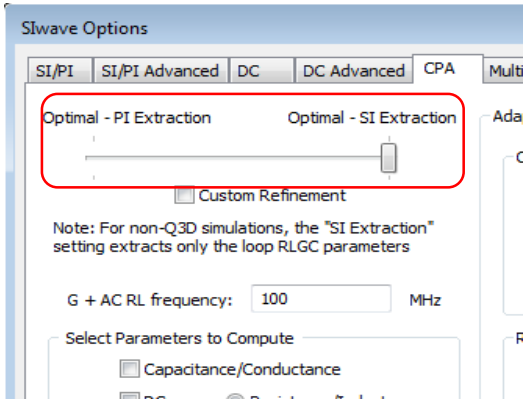


Step-3



IBIS model not available for Individual Src/Snk setup

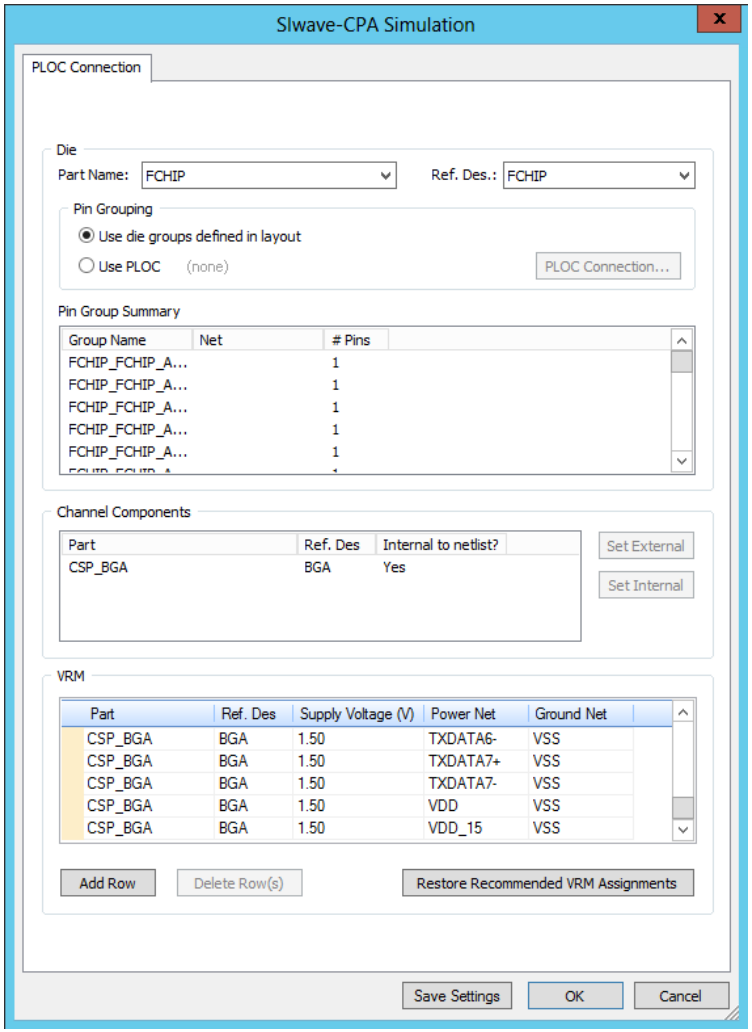




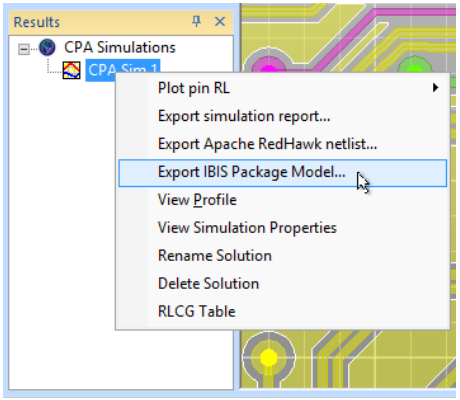
1) Net types do not matter. Nets can be set as Signal or PG types.
2) Group all the pins of each net on Die, and repeat on BGA.
3) Select VDD, VDD_15, VSS, and all DAT+ and DAT- nets.
4) Go to Other Solver settings and select “Exhaustive” from slidebar and from Net processing tab, choose “Use current net selection for simulation”.

Select “SI Extraction” option to get better accuracy for SI problems and also to compute loop-based RLCG data needed for IBIS.

Package IBIS Model Generation



5) Set FCHIP as the Die component, and CSP_BGA as VRM.
6) Start the simulation.
7) Once the simulation is done, RLCG table can be viewed, and the IBIS model can be exported.



0001_CPA_Sim_1.pkg

```
[IBIS Ver]                5.0
[Comment Char]            |_char
[File Name]               0001_CPA_Sim_1.pkg
[File Rev]                1.0
[Date]                    Fri Aug 12 11:54:53 2016

[Source]                  From Ansys Inc.' result.
[Notes]
[Disclaimer]
[Copyright]
|
[Define Package Model]    0001_CPA_Sim_1
[Manufacturer]            unknown
[OEM]                     unknown
[Description]             unknown
|
[Number Of Pins]          35
|
[Pin Numbers]
| Pin Name Terminal        Net Name     Starting Node       Ending Node
   B18   |     1           RXDATA0+   FCHIP_FCHIP_n237   CSP_BGA_BGA_n674
   C18   |     2           RXDATA0-   FCHIP_FCHIP_n236   CSP_BGA_BGA_n673
   E18   |     3           RXDATA1+   FCHIP_FCHIP_n232   CSP_BGA_BGA_n669
   D18   |     4           RXDATA1-   FCHIP_FCHIP_n233   CSP_BGA_BGA_n670
```

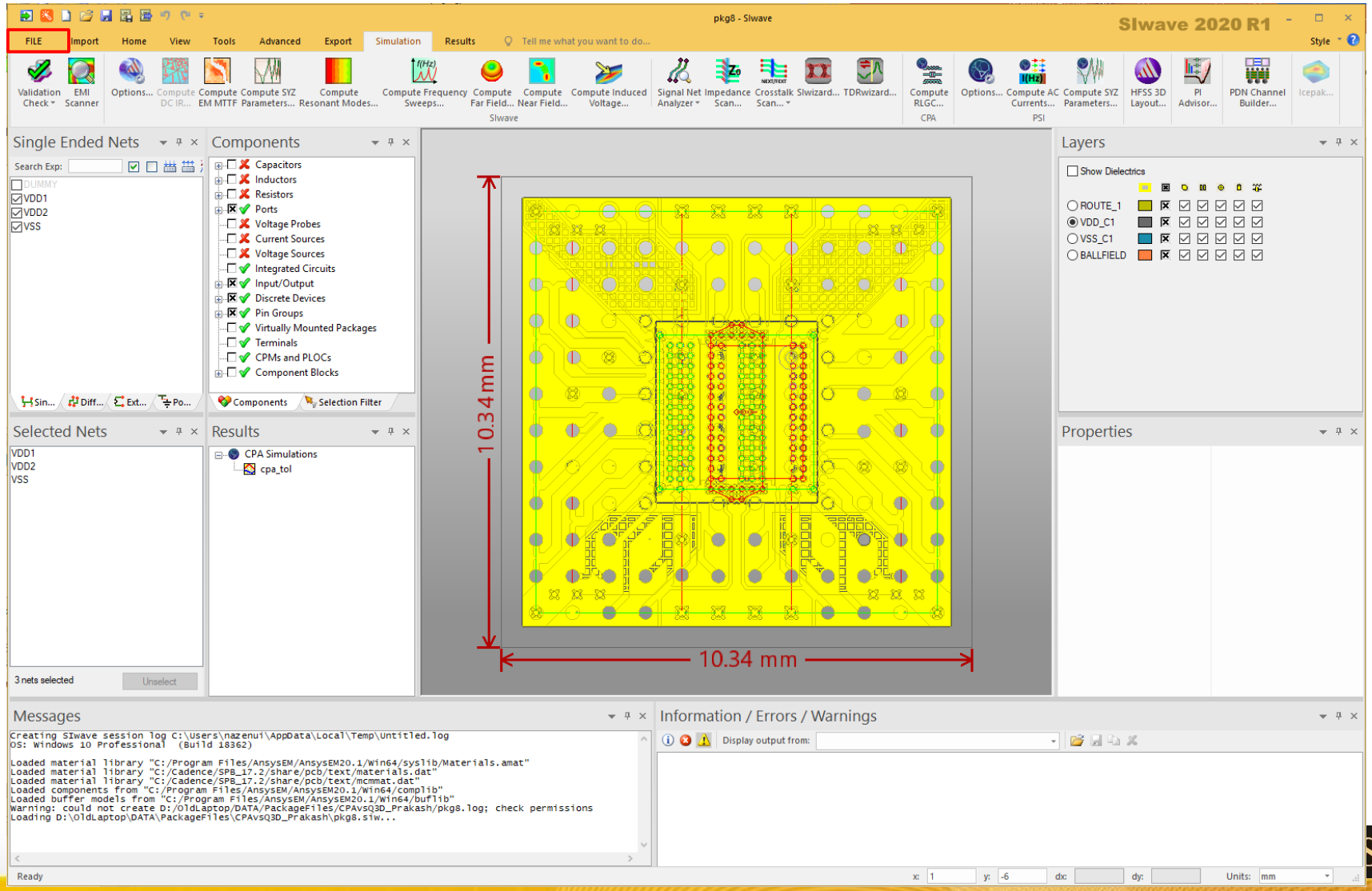
IBIS .pkg model

Key Setup Guidelines

- For simulation performance & accuracy, **classify various nets properly**
  - Large planes as Power/Ground nets
  - Signal Nets as Non-Power/Ground nets
- Define solderballs and solderbumps for appropriate padstacks
- Define Pin Groups as needed
- **SIwave** (see example projects for details)
  - **Tools -> Sanitize Layout** to clean up planes and traces #1
  - **Simulation -> Validation Check** to identify and fix any problem areas #2
  - **Simulation -> Compute RLGC (CPA)** -> select either **Individual Source/Sink** or **CPA channel** setup,
    - **Individual source/sink setup**-- user defines source/sink per pin or pin group
    - **CPA Channel setup** – user specifies Die, Channel components, VRM
  - Set **Extraction Type: RLCG Model** only -> **CPA** fast FEM; **Q3D Solver** -> MoM Solver
  - Under **Other Solver Settings,** setup **Netprocessing**, **Multiprocessing, CPA** options
  - **Run analysis** & **post-process** results

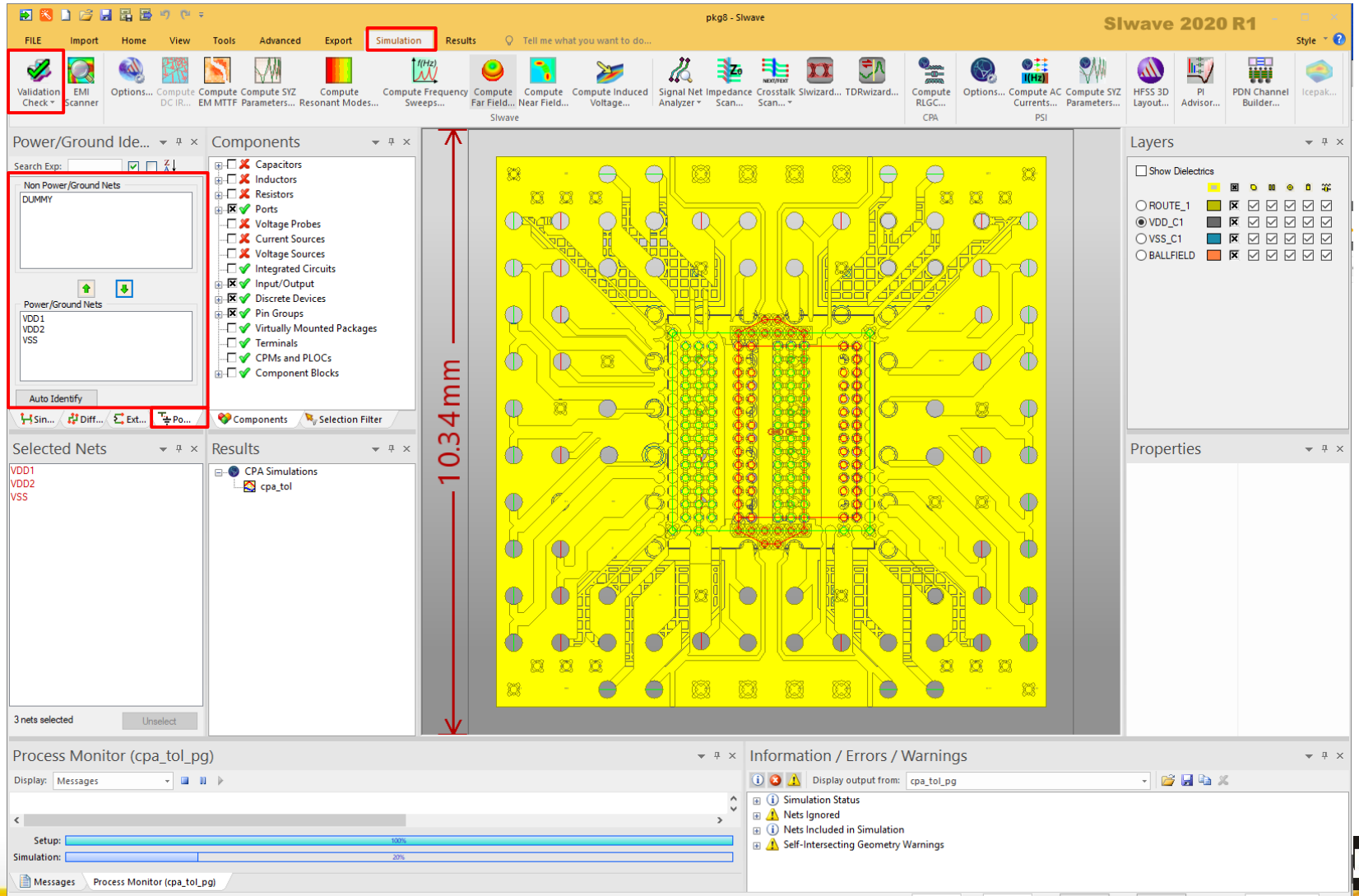
Example 1- Package PDN extraction

- Open project file **pkg.siw** : **SIwave** -> **File** -> **Open** -> Browse to file location



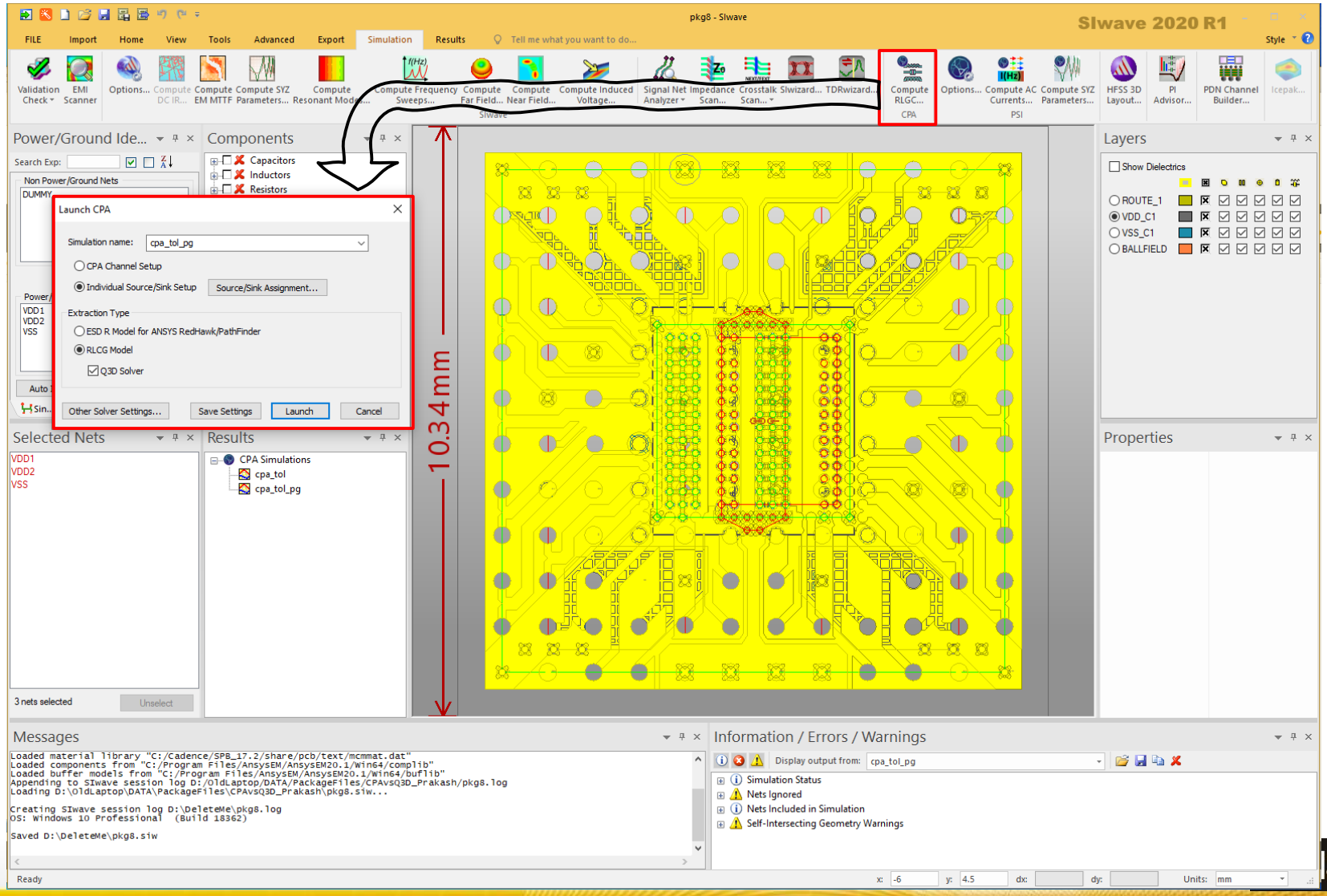
Example 1- Package PDN extraction

- Classify **Power/Ground Nets** accordingly
- **Tools -> Sanitize Layout**
- **Simulation -> Validation Check**



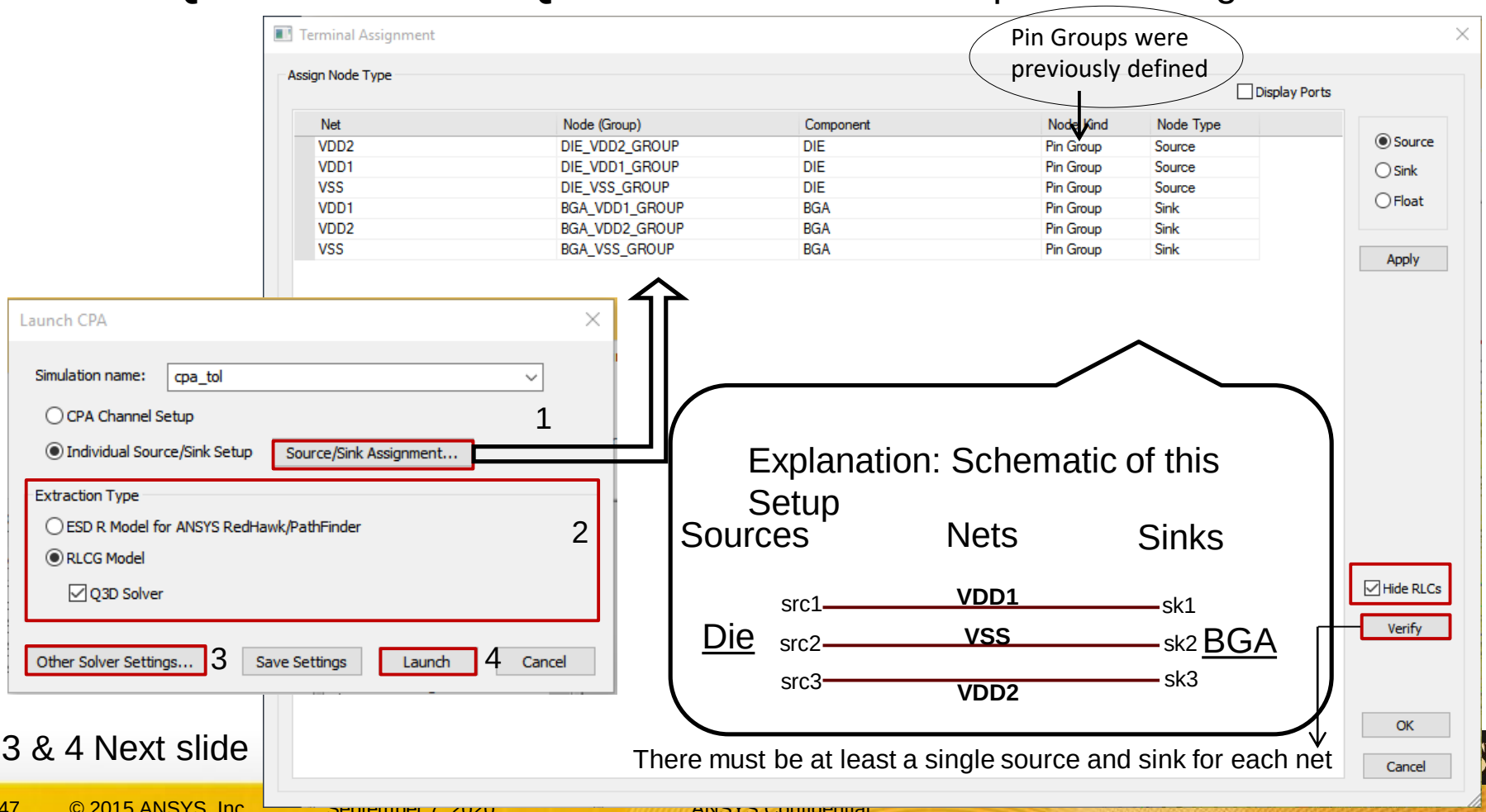
Example 1- Package PDN extraction

- Launch CPA interface: **Simulations -> Compute RLGC (CPA)**



Example 1- Package PDN extraction

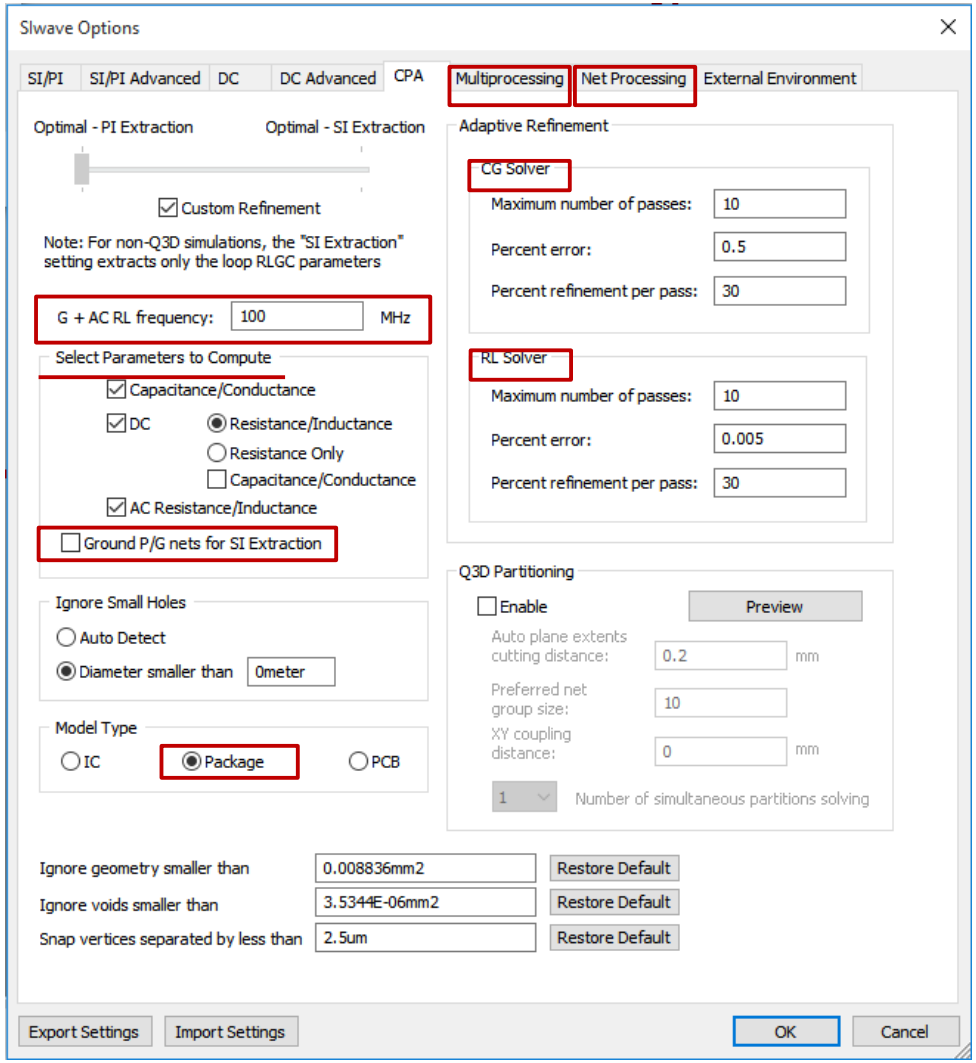
- Select **Individual Source/Sink Setup** option
- Click on the **Source/Sink Assignment** button, & assign **Node Type** as below
- Set **Extraction Type** (**select RLCG Model+Q3D Solver** for this example)
  - **RLCG Model** only -> **CPA** fast FEM
  - **Q3D Solver** -> Use **Q3D** MoM Solver with Adaptive Meshing



3 & 4 Next slide

Example 1- Package PDN extraction

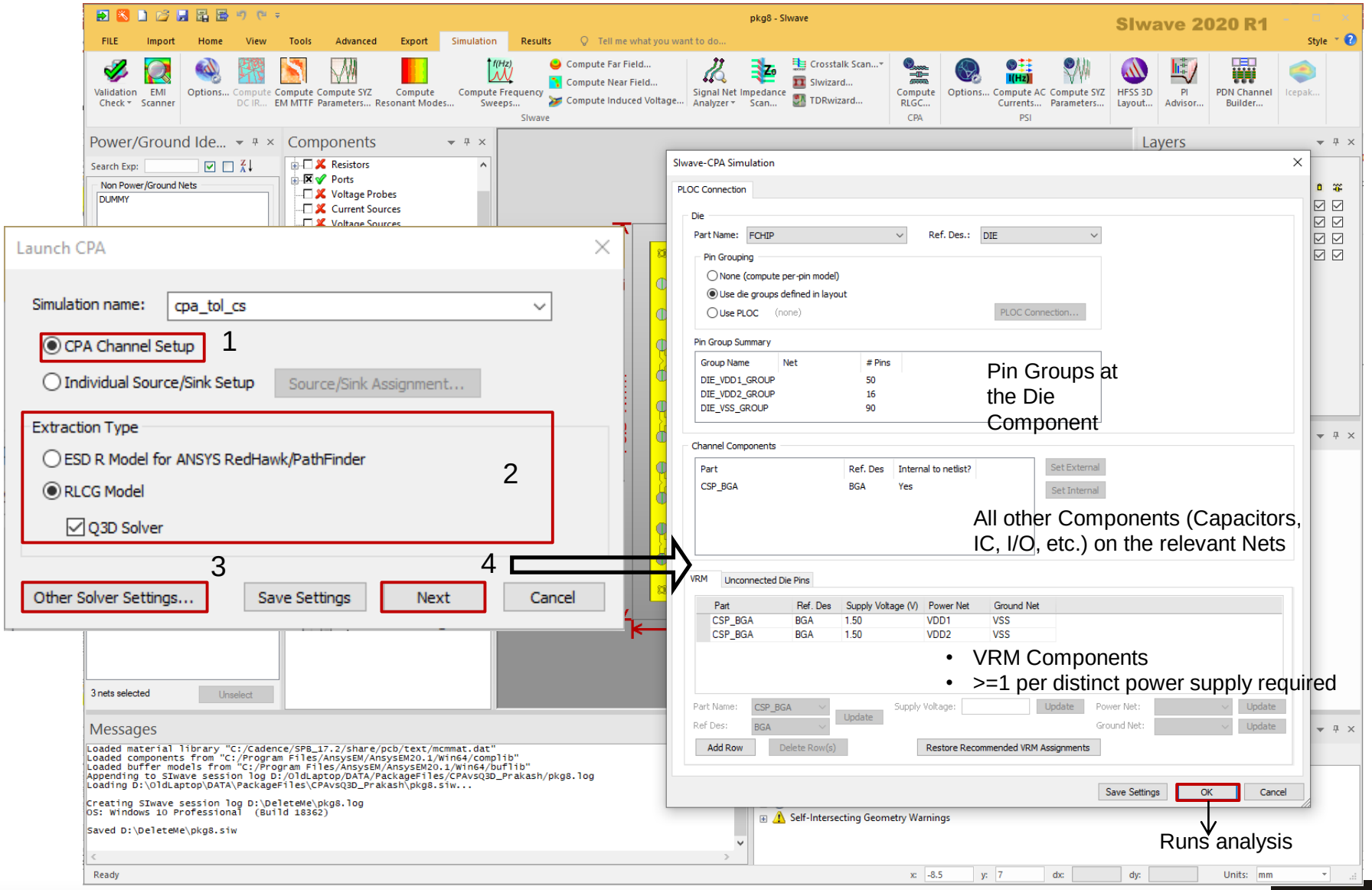
- CPA Setup – **Other Solver Settings** & **Launch** simulations



- Under Net Processing, choose either custom or auto net selection
- Choose **Custom Net Selection** to include only Nets in the **Selected Nets** window in the simulation
- Specify AC solution frequency as **G+AC RL Frequency**
- Select desired **Parameters to Compute**
- Adjust **CG solver** and **RL solver** convergence settings
- Use **slider bar** for recommended settings for either SI or PI extraction
- Set Model Type to **IC** for RDL structures and **Package** or **PCB** for others
- In the **Multiprocessing tab**, set available #cores & HPC license
- The CPA setup options can be **exported** for subsequent reuse

- OK to complete setup. **Launch** Simulation

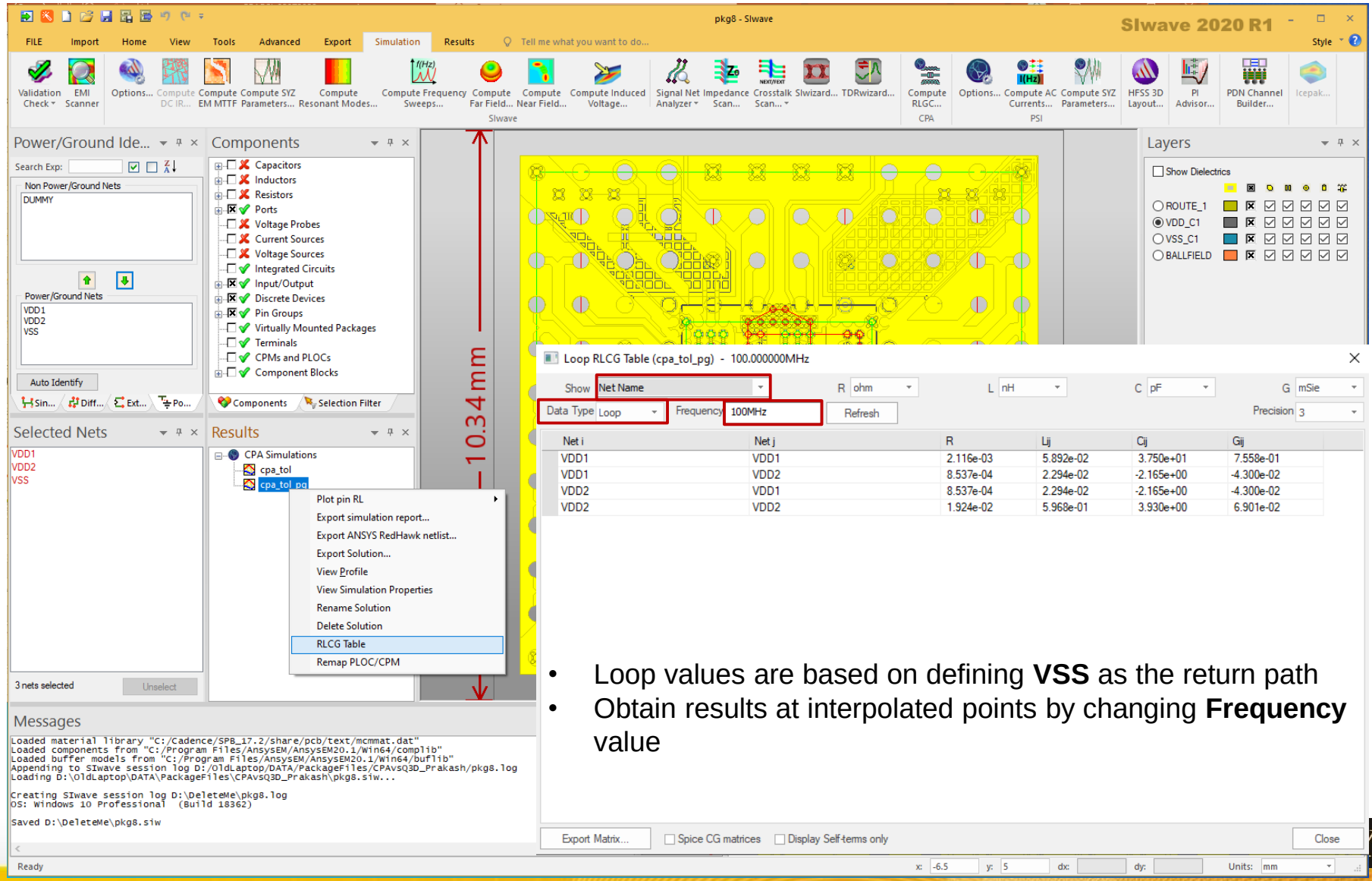
Optionally, **CPA Channel Setup** Option



- **CPA Channel Setup** requires that all the components have the reference net (usually ground net) routed to them

Example 1- Package PDN extraction

- Simulation Results – Partial and Loop RLCG values are generated
- RMC on the **Results folder** -> RLCG Table, Show **Net Name,** Data Type **Loop** – see below



- Loop values are based on defining **VSS** as the return path
- Obtain results at interpolated points by changing **Frequency** value

Simulation Results for various Solvers

SIwave **RLCG Model** Only -- aka **CPA fast FEM**

Net i	Net j	Rij (mΩ)	Lij (nH)	Cij (pF)	Gij (mSie)
VDD1	VDD1	2.081	0.06831	32.39	0.6682
VDD2	VDD2	24.260	0.4602	3.755	0.06701

SIwave **RLCG Model** +**Q3D Solver** -- aka **CPA MoM**

Net i	Net j	Rij (mΩ)	Lij (nH)	Cij (pF)	Gij (mSie)
VDD1	VDD1	2.107	0.05892	35.700	0.75420
VDD2	VDD2	19.210	0.59680	3.717	0.06754

Q3D Standalone

Net i	Net j	Rij (mΩ)	Lij (nH)	Cij (pF)	Gij (mSie)
VDD1	VDD1	2.0466	0.054864	36.153	0.76444
VDD2	VDD2	17.716	0.57016	3.741	0.067852

Comments

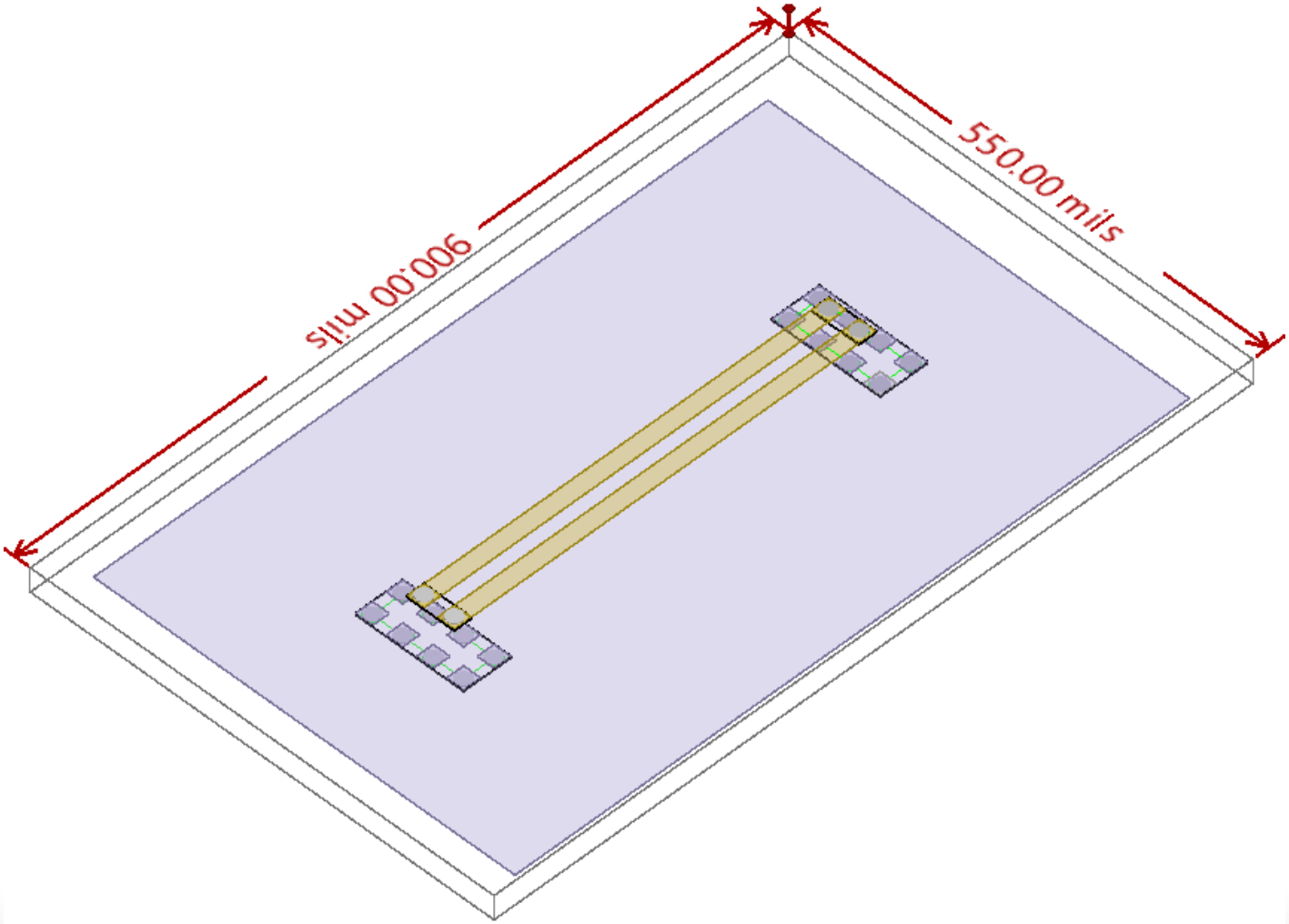
Total: 0m53s Fastest & Accurate

Total: 14m44s Fast & More Accurate

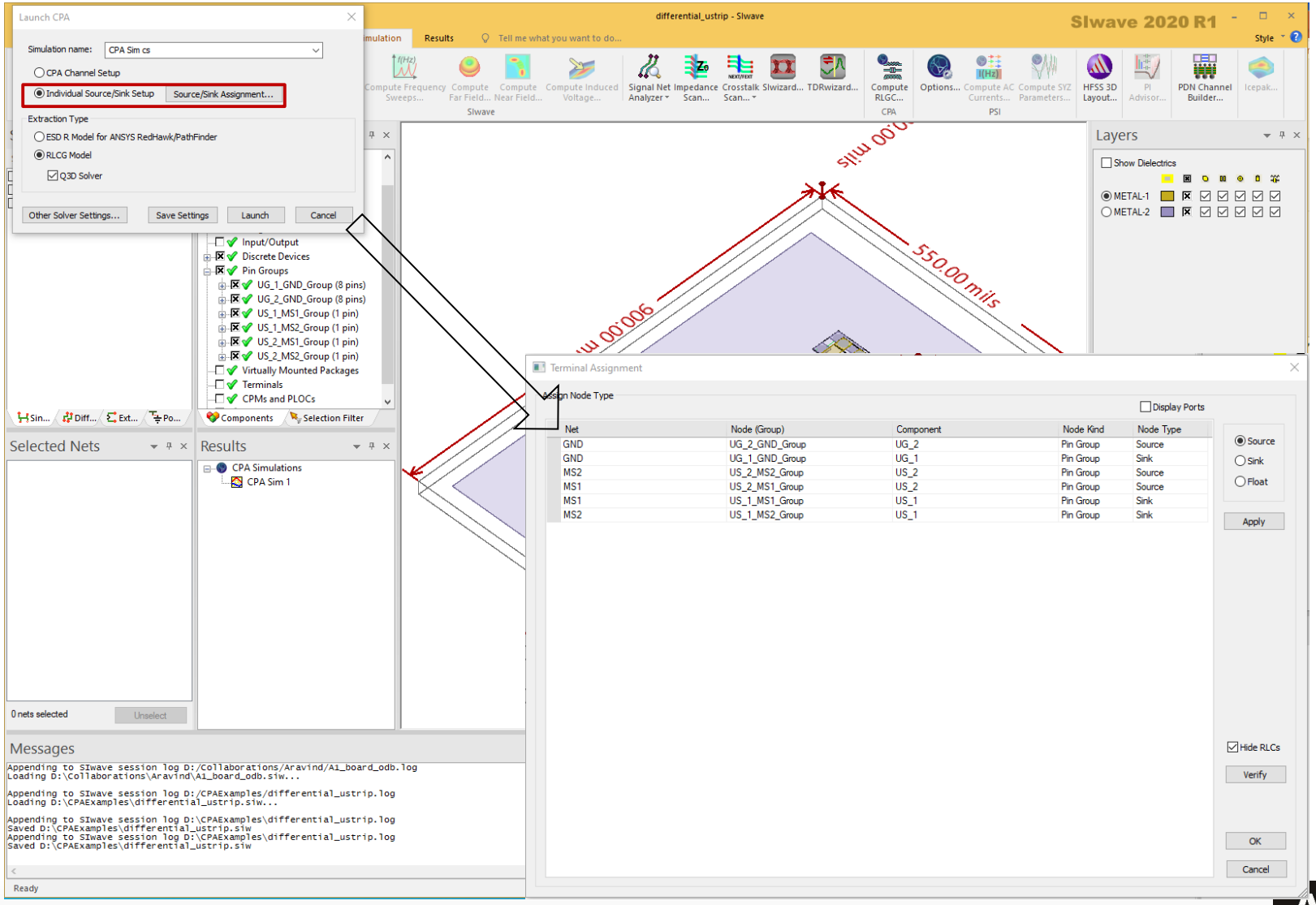
Total: 51m12s Standard for Accuracy

Example 2: Differential Pair Example

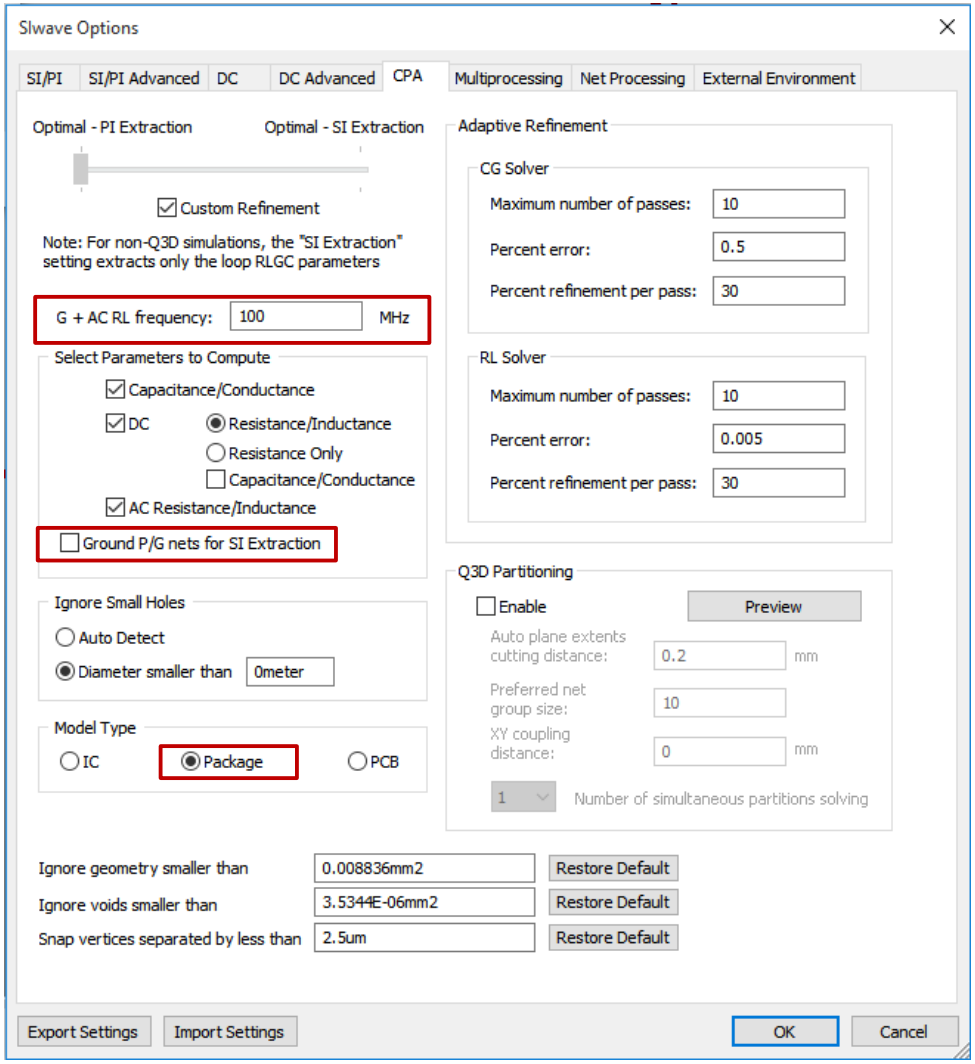
- Open project file **differential_ustrip.siw**
- **Slwave** -> **File** -> **Open** -> Browse to file location



- Select **Individual Source/Sink Setup** -> **Source/Sink Assignment** and setup sources and sinks as shown below

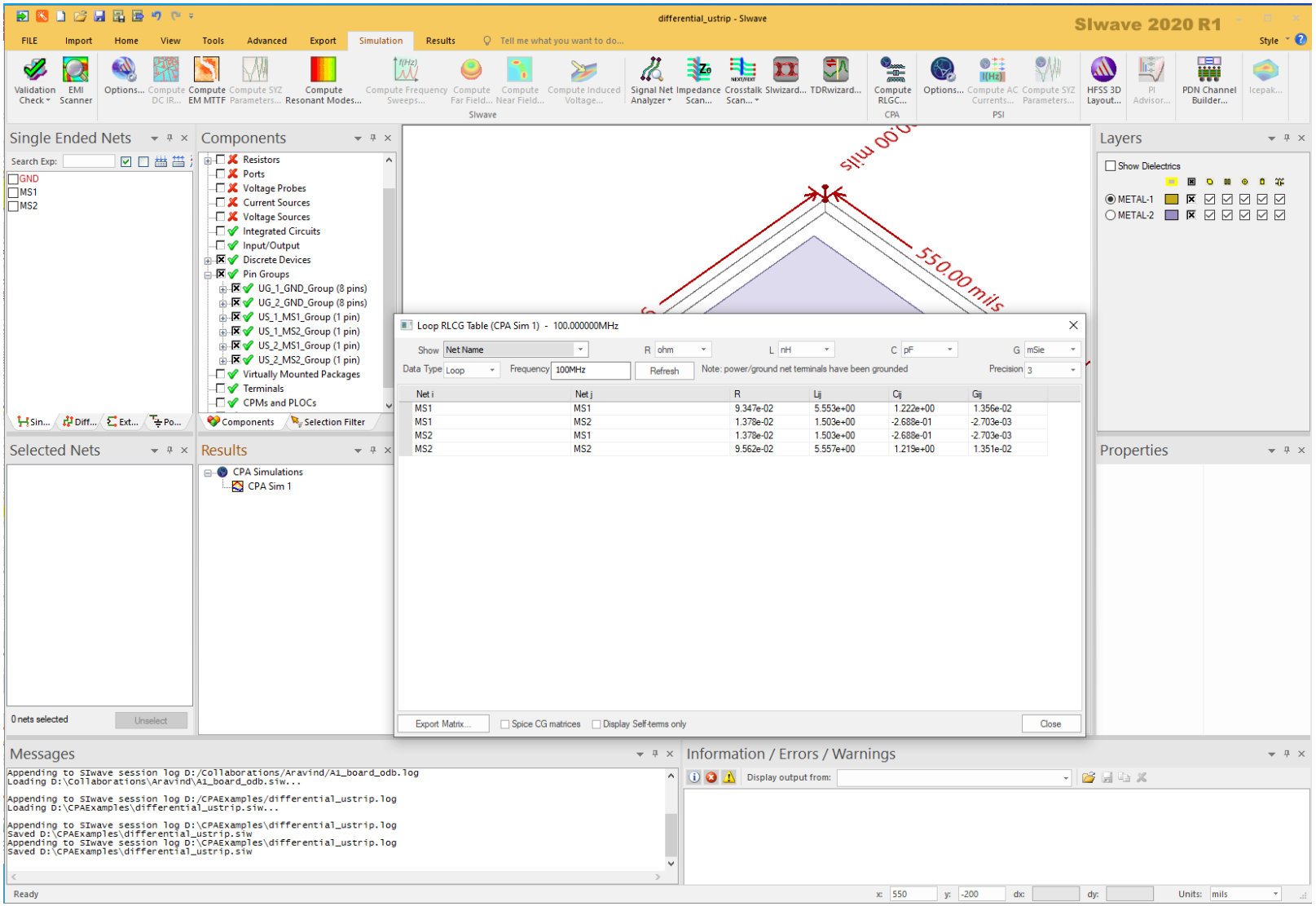


- Launch **Other Solver Settings** and configure the options – see below
- Setup the **NetProcessing** (choose **auto** option) & **Multiprocessing** tabs



- OK to complete setup. **Launch** Simulation

Simulation Results & Interpretation

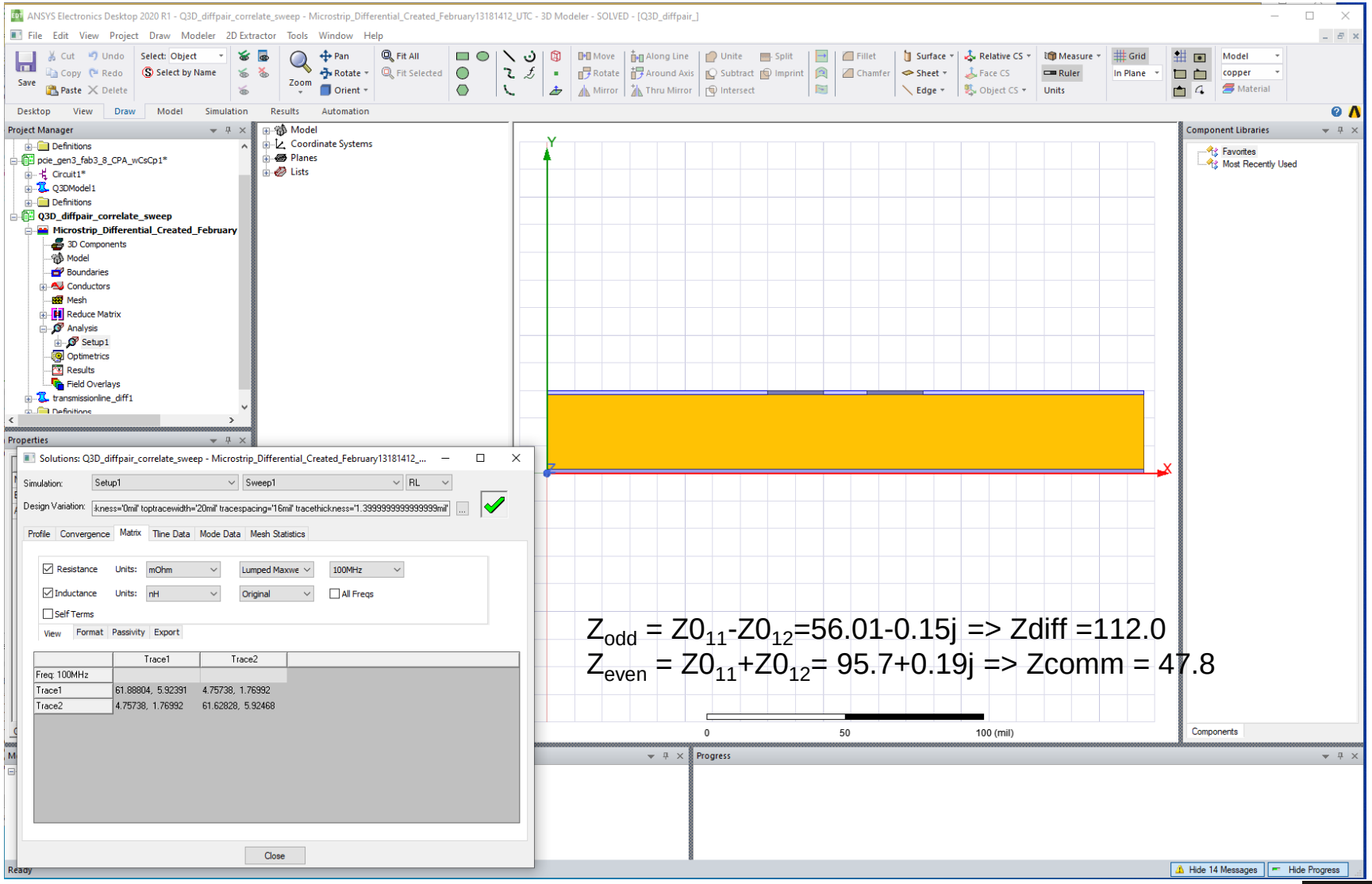


$Z_{odd} = sqrt{(L_{11}-L_{12})/(C_{11}-C_{12})} = 52.12 \Rightarrow Z_{diff} = 2*Z_{odd} = 104.24$

$Z_{even} = sqrt{(L_{11}+L_{12})/(C_{11}+C_{12})} = 86.04 \Rightarrow Z_{comm} = (1/2)*Z_{even} = 43.02$

Comparison with 2D Extractor

- Run the 2D Extractor simulation included and review the results



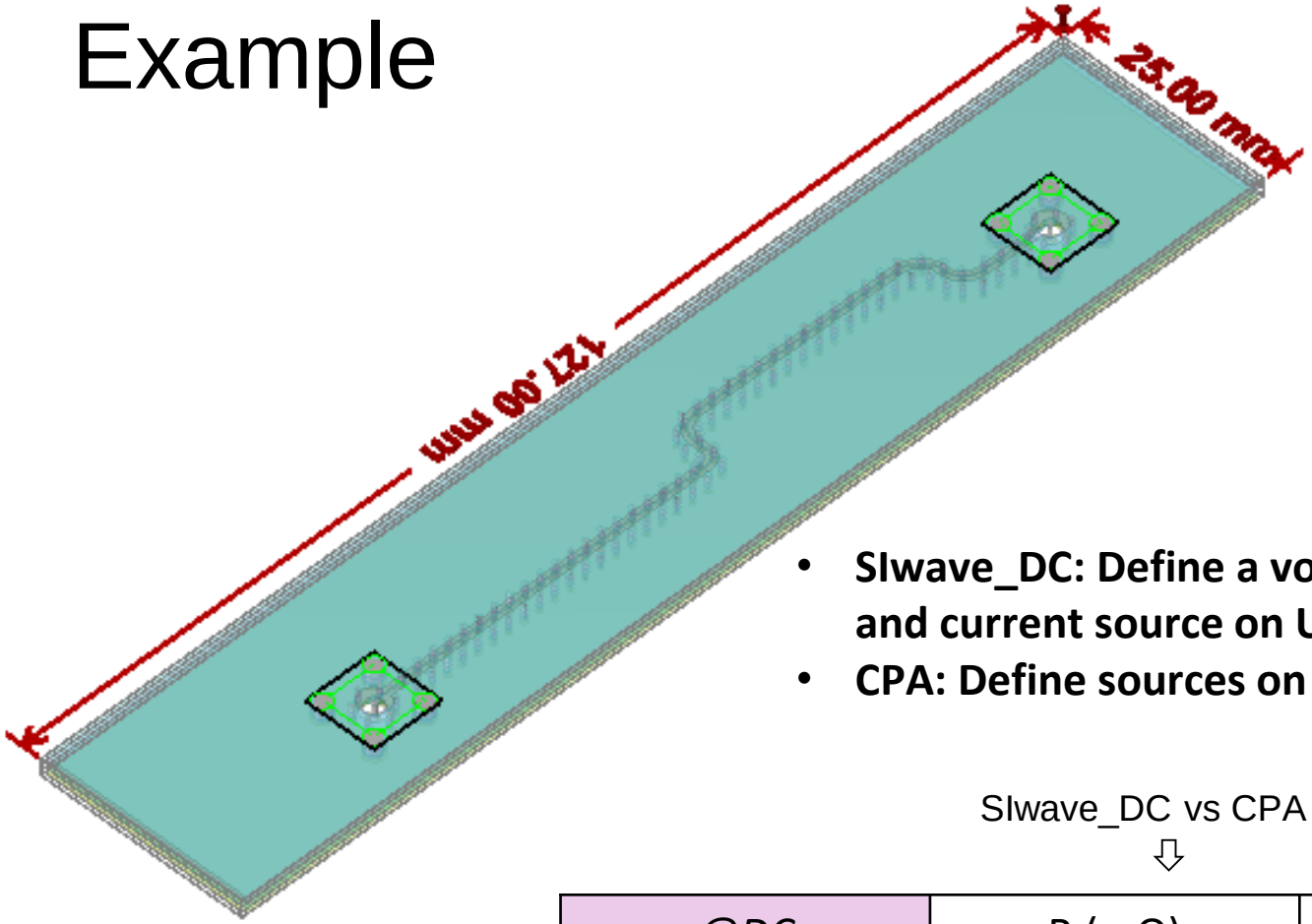
- Comparing 2D Extractor vs Q3D results Zdiff = 112.0 vs 104.2 and Zcomm = 47.8 vs 43.0

Conclusion of 2D Extractor vs Q3D

For this example

- The difference in results between 2D Extractor and Q3D in this example is due to the edge effects that exist in the Q3D model
- Remember that the 2D Extractor extract the per-unit-length parameters assuming an infinitely long transmission line

Extra: Transmission line Extraction Example



- **SIwave_DC: Define a voltage source on U10 and current source on U11**
- **CPA: Define sources on U10 and sinks on U11**

SIwave_DC vs CPA

⇩

@DC	R (mΩ)	L (nH)
SIwave DC	158.39	78.29
CPA	158.30	78.13