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SANECHIPS™

Ansys INNOVATION CONFERENCE 2020

Challenges and Solutions of PI Signoff for Next Generation Large Scale Chips with TSMC 7nm Process Technology

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ZTE SANECHIPS

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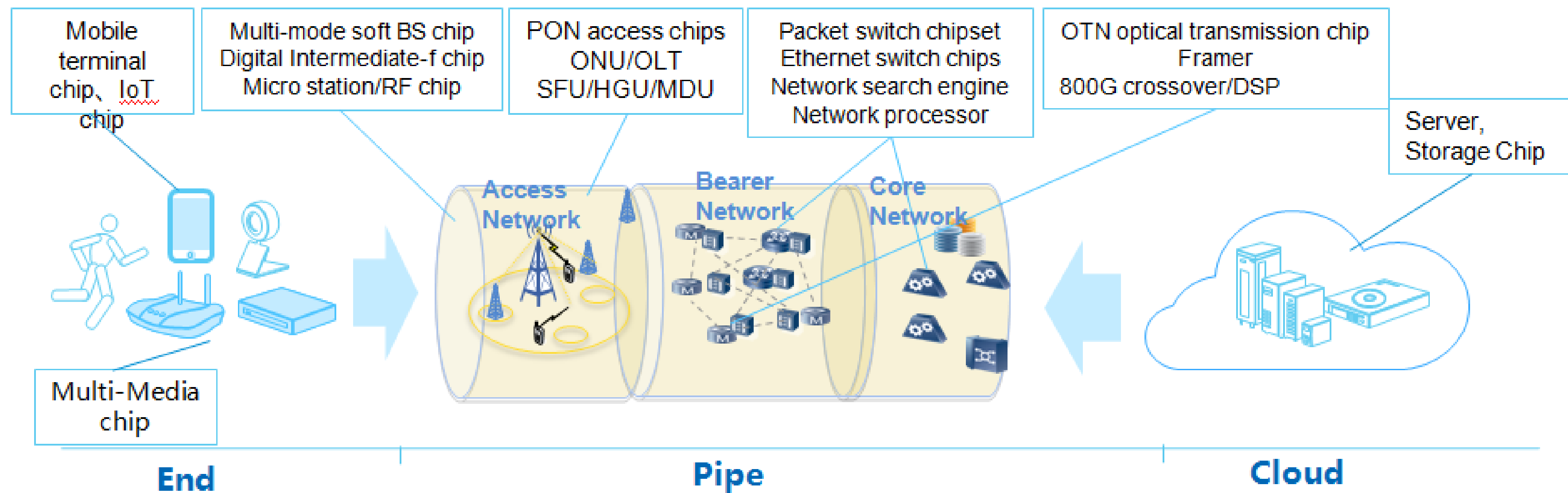
General Overview of Sanechips

- 20+ years in IC developments Re-organized as an independent legal entity in 2003
- Leading Chip provider in industry with 1800+ employees in 8 R&D centers
- Advanced physical design capability with cutting-edge process technology
- 100+ chips in mass production, with board portfolio covering cloud, pipeline and terminals
- 3500+ patents owned including 1700+ international patents



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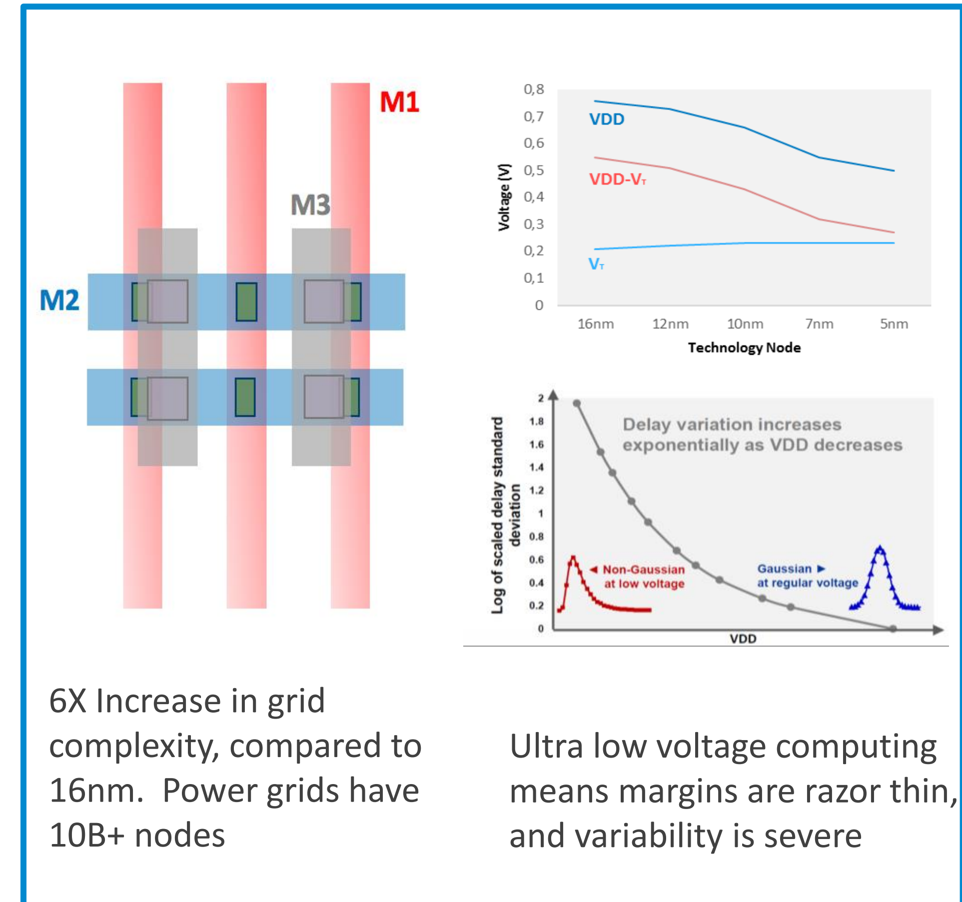
Backgrounds and Motivations

- **Design challenges on IREM**
  - ✓ **Evolution process technology**
    - ➢ Decreasing supply voltage
    - ➢ Demanding PVT corner coverage due to reduced PI noise margin
    - ➢ Significant self-heating effect
  - ✓ **Increasing design scale and complexity**
    - ➢ Single machine needs larger memory
    - ➢ Legacy multi-threads solution cannot meet PI simulation requirements
    - ➢ More functional scenes need to be simulated
    - ➢ Vector-based PI simulation becomes more and more difficult
- **Challenges in IREM signoff**
  - ✓ Resistance,nodes and local power density are increasing
  - ✓ The accuracy of vector selection becomes increasingly difficult
  - ✓ Accuracy of power calculation becomes increasingly important
  - ✓ Highly parallel elastic computing capabilities is critical to design cycle reduction



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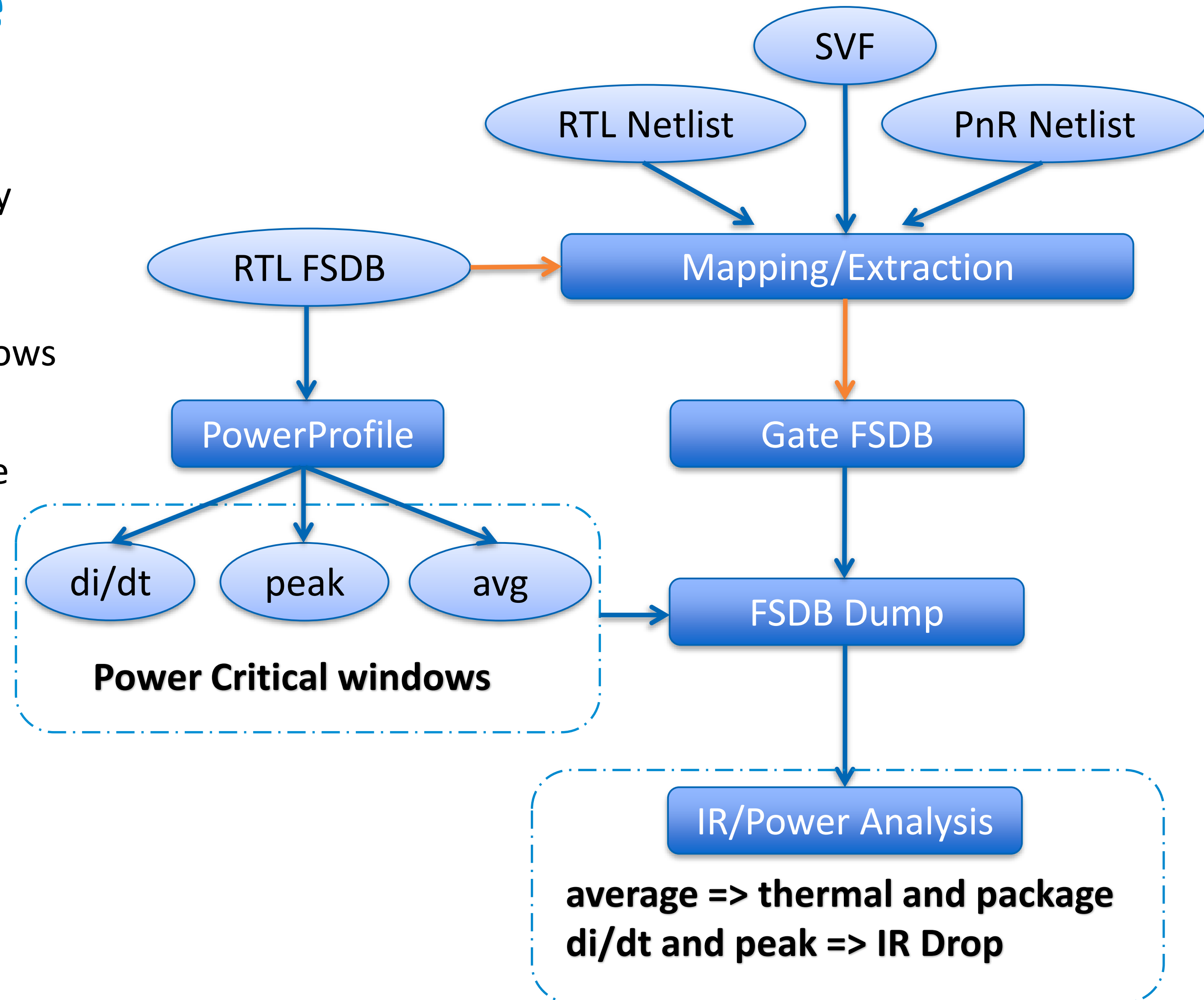
Solutions of Vector Coverage

- **Power-critical windows identification**
  - ✓ FSDB longer than 750us can be analyzed quickly with profile power(100x-1000x faster than per-cycle power)
  - ✓ Easy to identify peak and big di/dt power windows
- **Fast waveform conversion**
  - ✓ Significantly reduce GATE-FSDB generation time
  - ✓ Solve the pain-point of large vector generation

	RTL	postSim	RTL2GATE
FSDB length	750us	750us	750us
run time	1h	12h	0.4h



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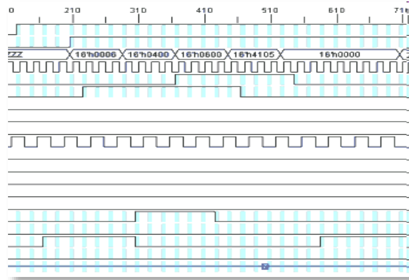
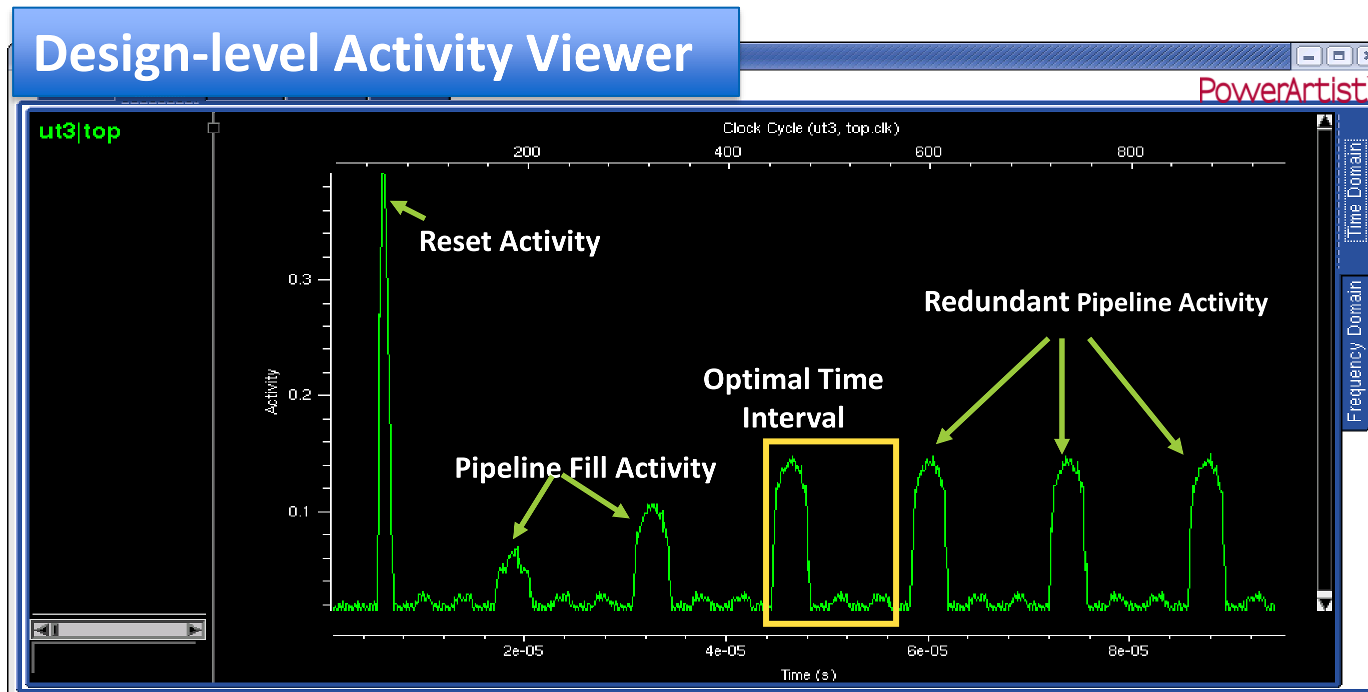
Profile Design Activity

- Conventional signal activity viewer



- Difficult to validate activity coverage
- Difficult to analyze activity per hierarchy



- Identify power-critical windows
- Qualify vectors per mode
- Identify wasted activity

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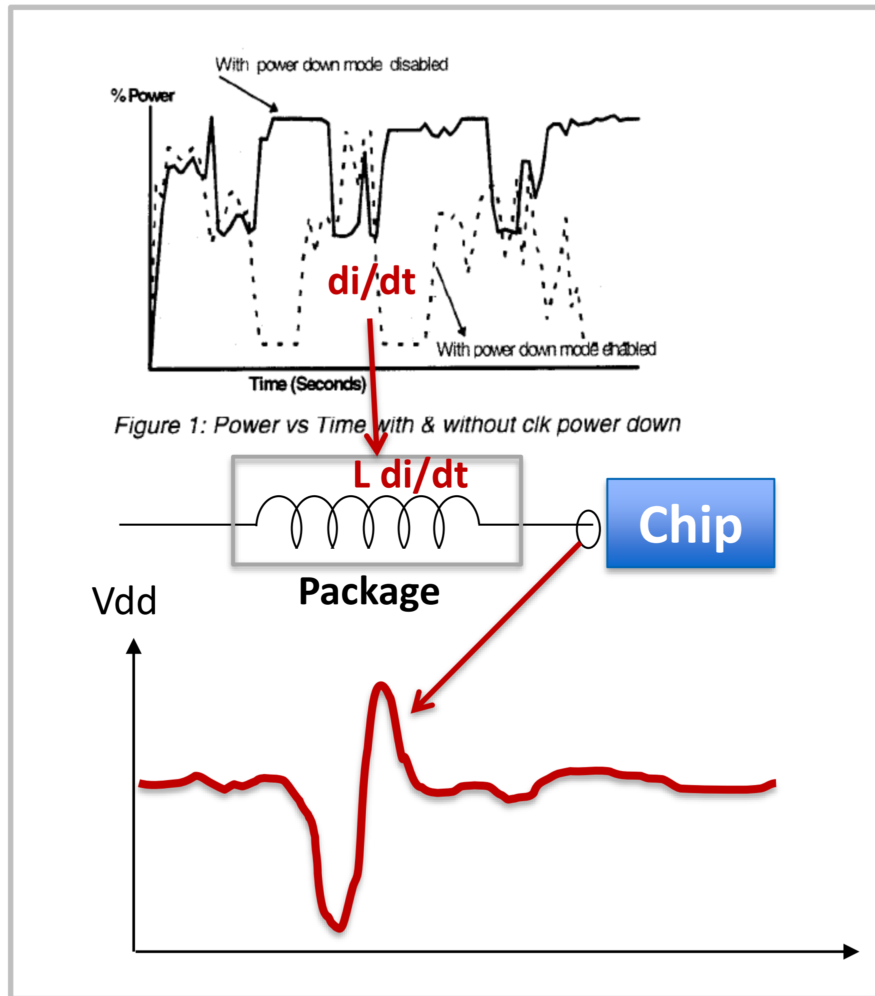
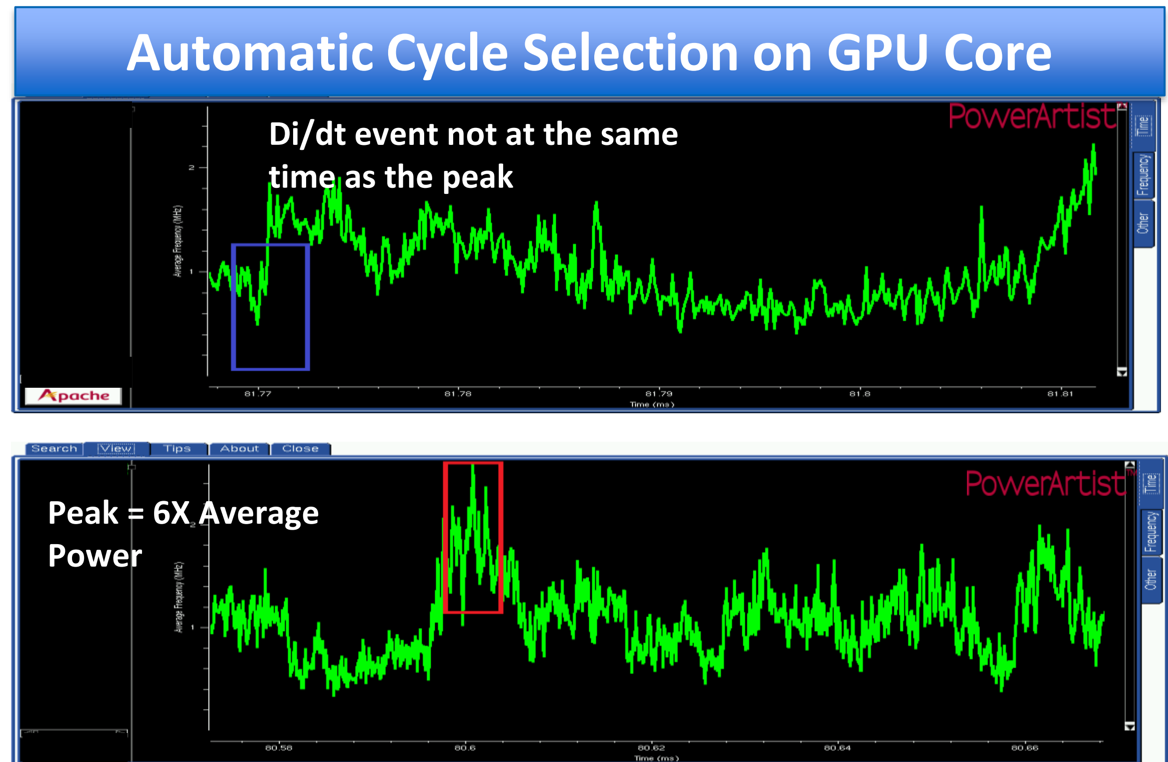
Power Critical Identification





- RTL provides high-performance for M+ cycles
- Can identify Peak and di/dt power-critical cycles
- Can directly interface to power grid integrity tool

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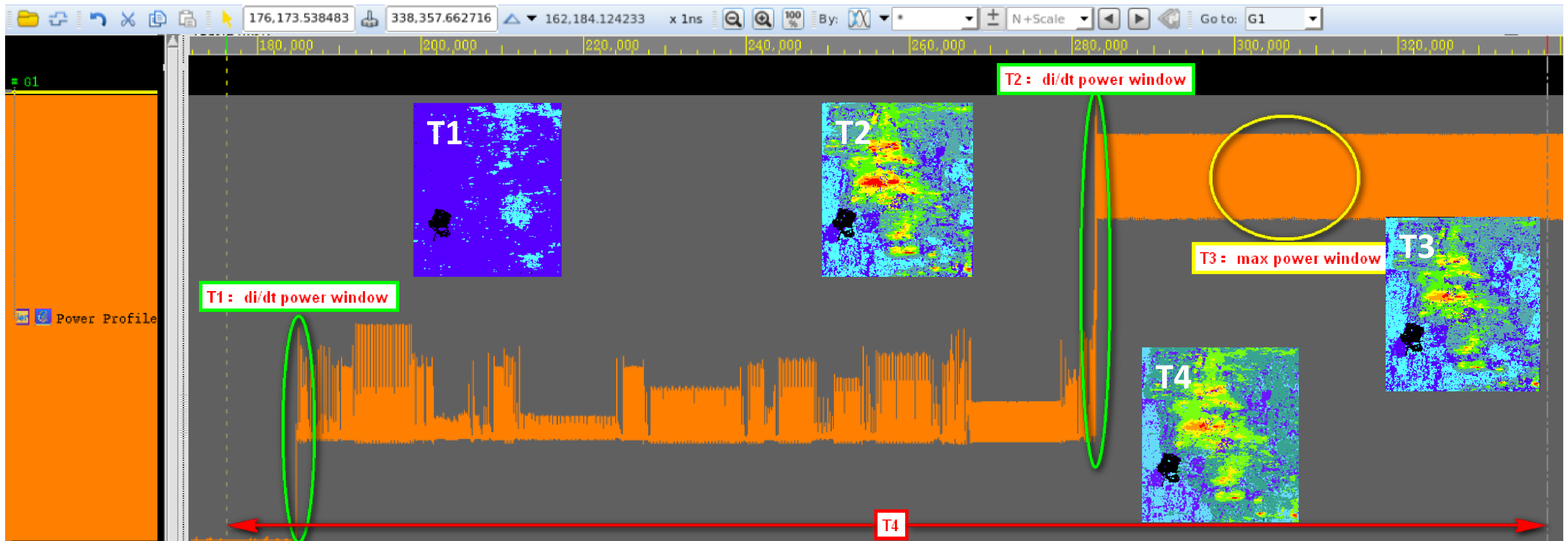
Power Profiling and Voltage Drop Results

- The di/dt and maxpower windows are important for PI analysis
- ProfilePower can quickly find the peak and the large di/dt windows



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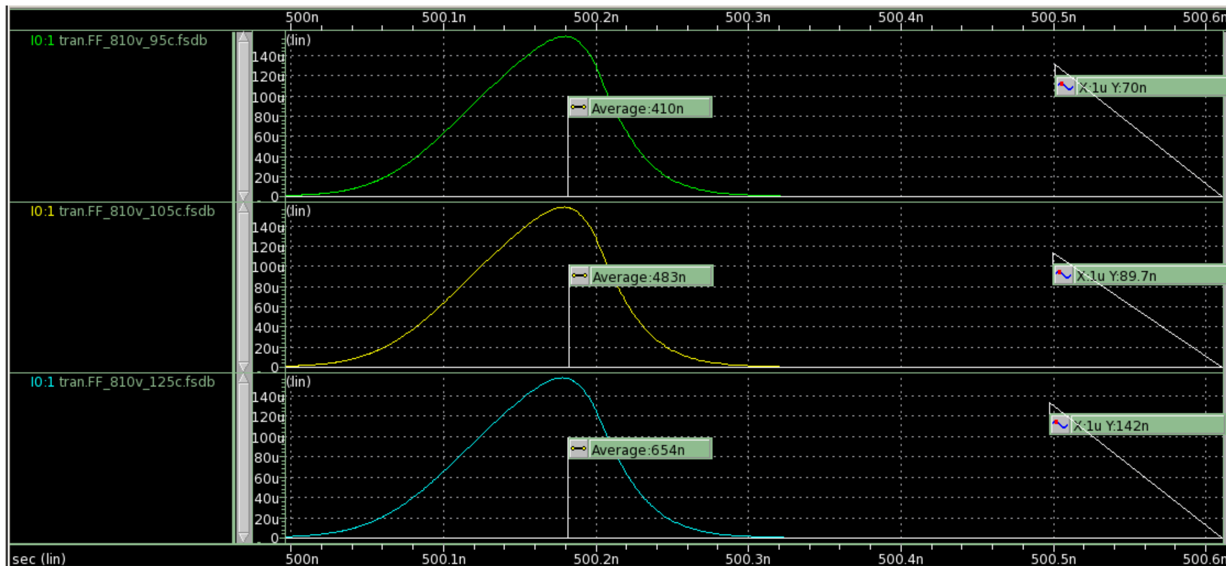
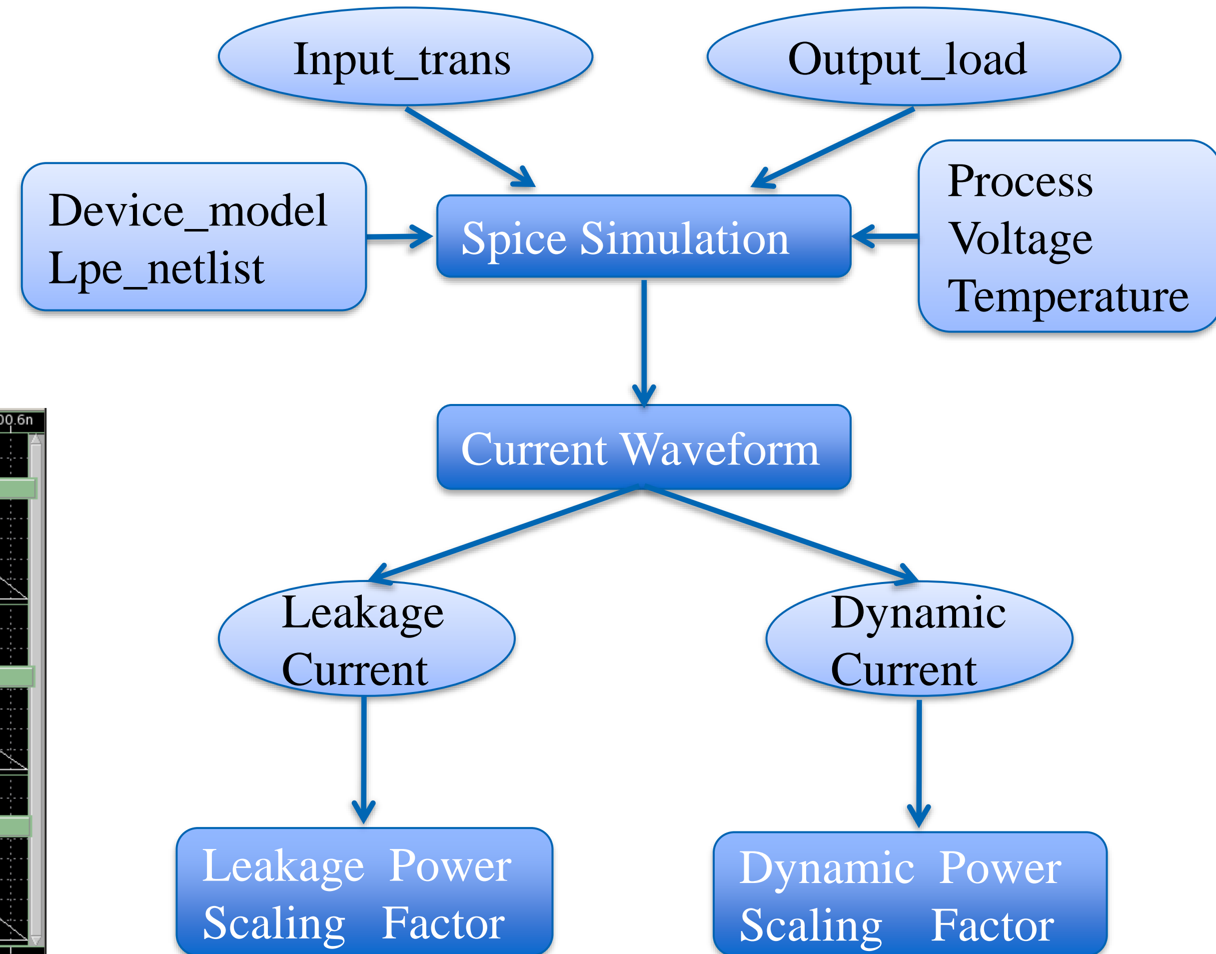
Solutions of Accurate Power Estimation

- Spice tools were used to calculate power of different process, voltage, temperature and frequency
- Matrix containing these power results were solved to get leakage power factor and dynamic power factor





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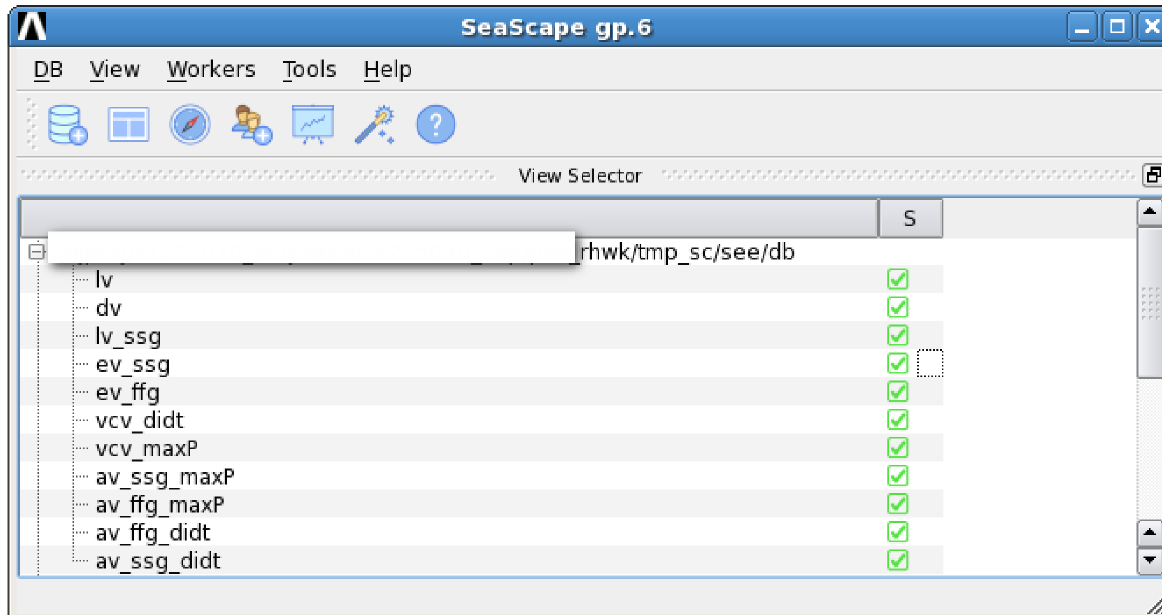
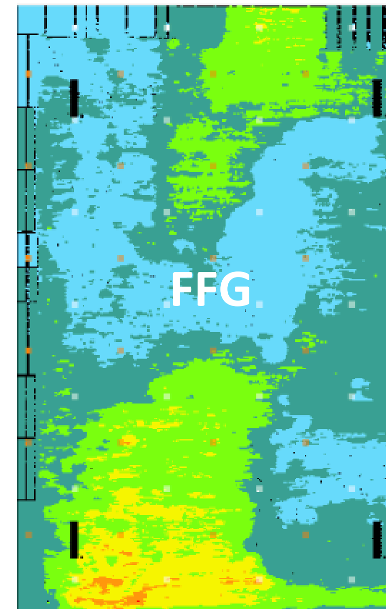
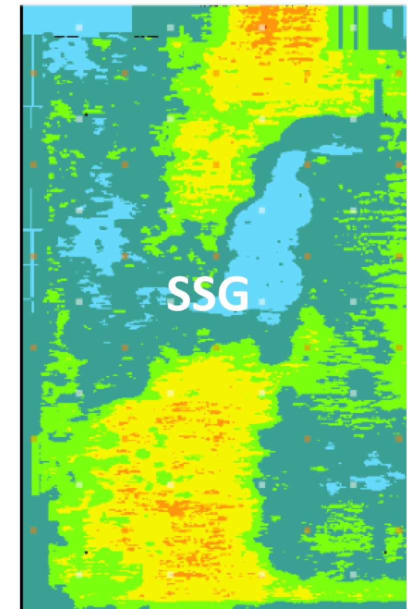
Corner Coverage of PI Analysis

- **FFG may not be the worst corner for PI analysis**
  - ✓ For signalEM analysis, m40C_rcbest_ccbest is more worst than 125C_cworst_ccworst
  - ✓ For dynamic voltage drop, FFG can't completely cover other PVT corners
- **Highly parallel elastic computing capability of RedHawk-SC**
  - ✓ Legacy multi-threads solution cannot meet PI simulation requirements
  - ✓ With RedHawk-SC's shared design view, Multiple RC(extraction view), vcd(value change view) can exist in a single db

	ML	LT
ML	no-violation	116.96%
LT	-	147.40%







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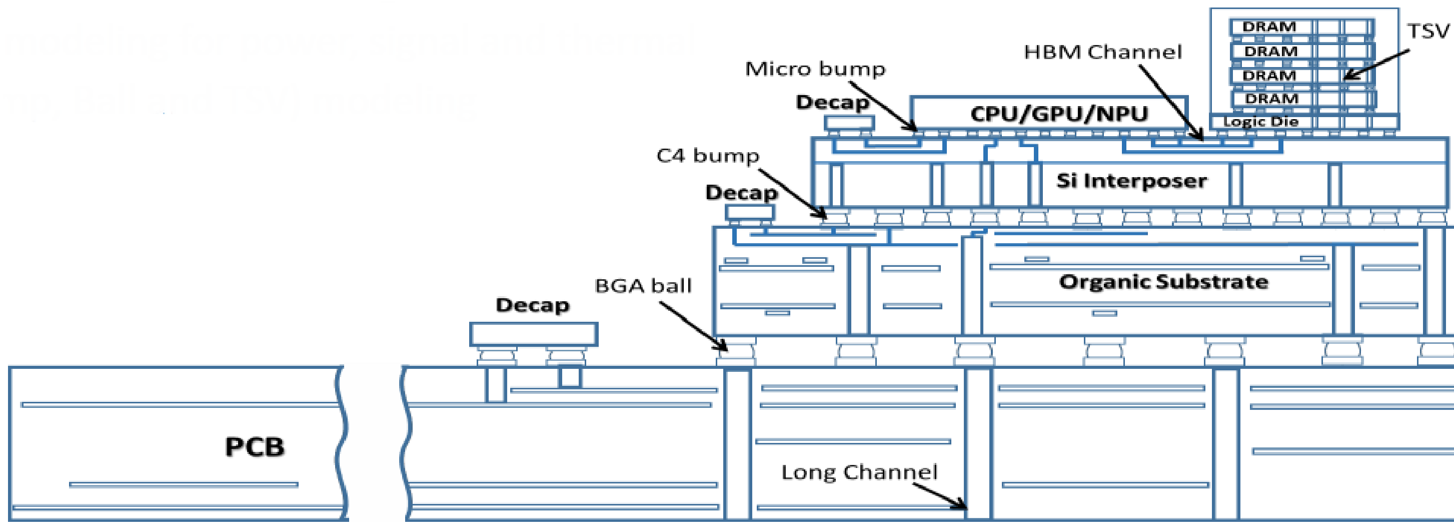
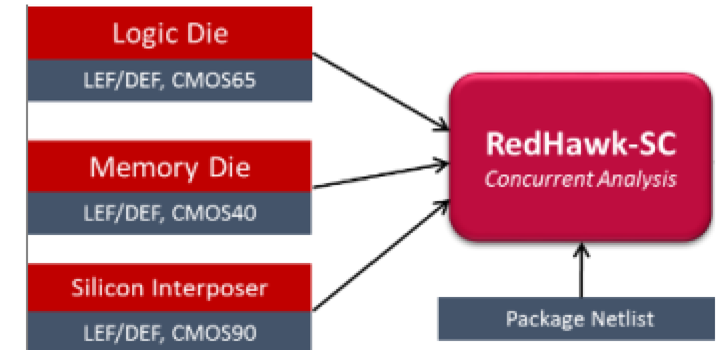
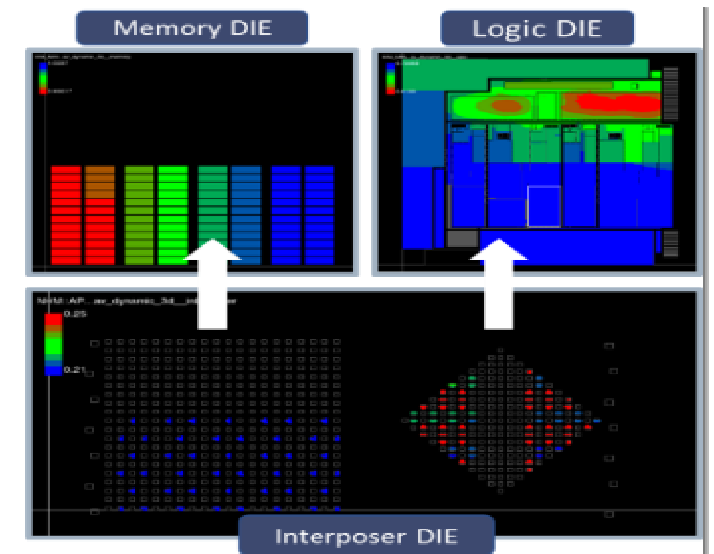
Concurrent 2.5D-IC Simulation







- High end applications, like AI, networking and HPC require high memory bandwidth, low power and extreme performance
- It's essential to run concurrent simulation to capture coupling noise between dies and interposer, especially for high-frequency signals

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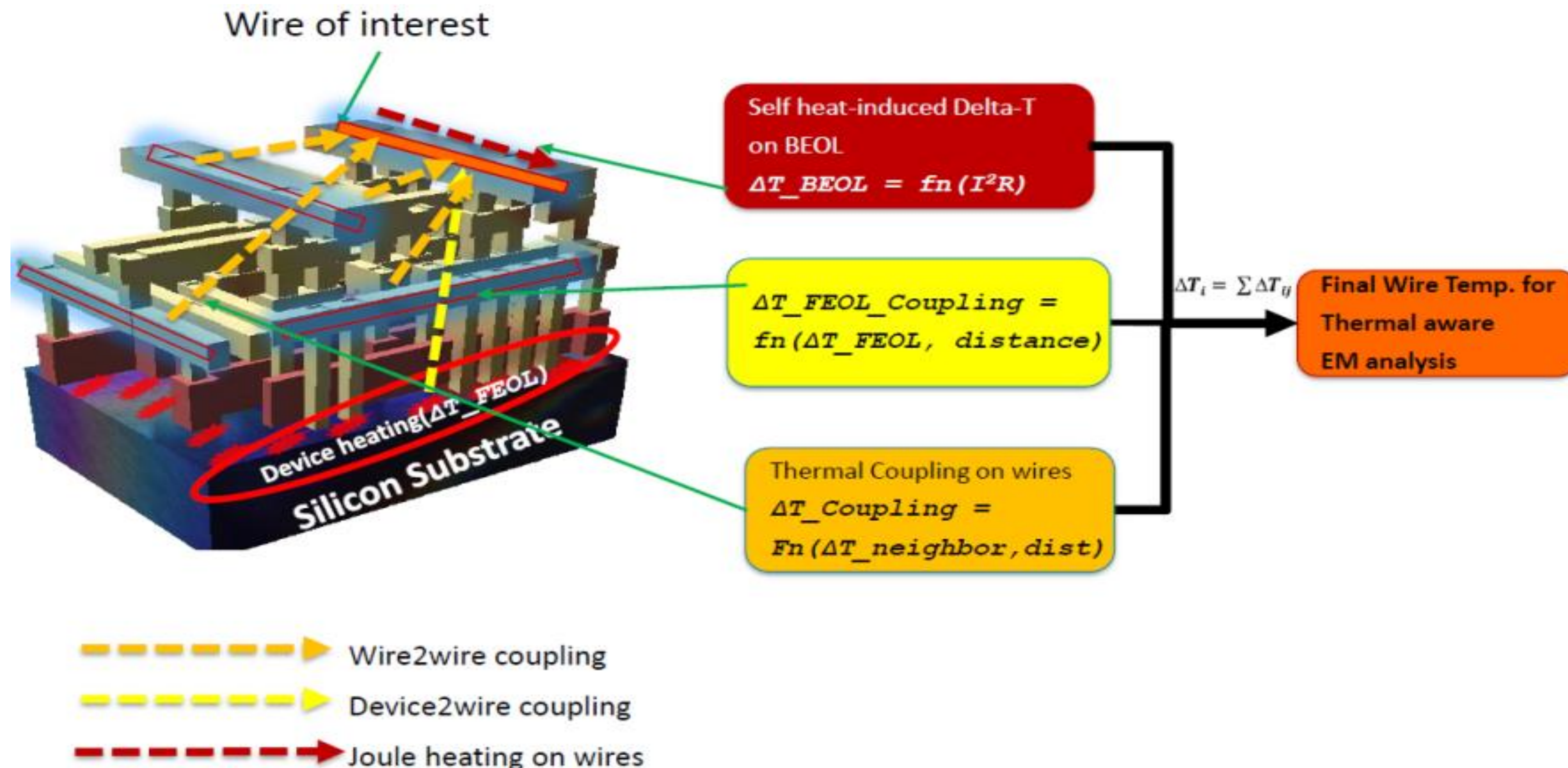
Thermal-Aware Statistical EM

- With narrow 3-D fin structure and lower thermal conductivity in substrate, local temperature on FinFET device can be higher than planar MOS device, which will degrade lifetime of interconnections significantly
- BEOL(wire/via) Joule heating, FEOL(device) Couple heating



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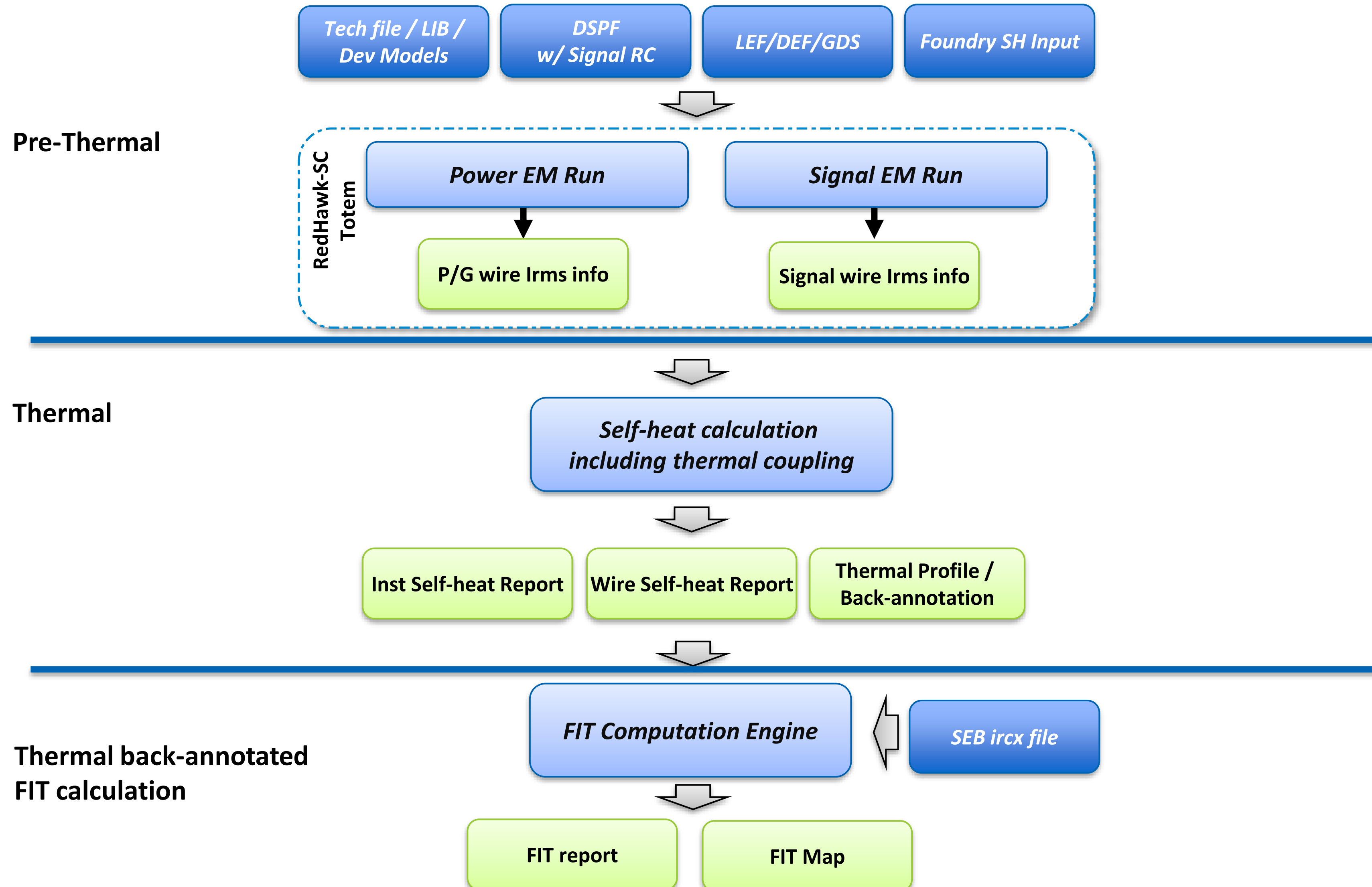
Thermal-Aware Statistical EM Flow



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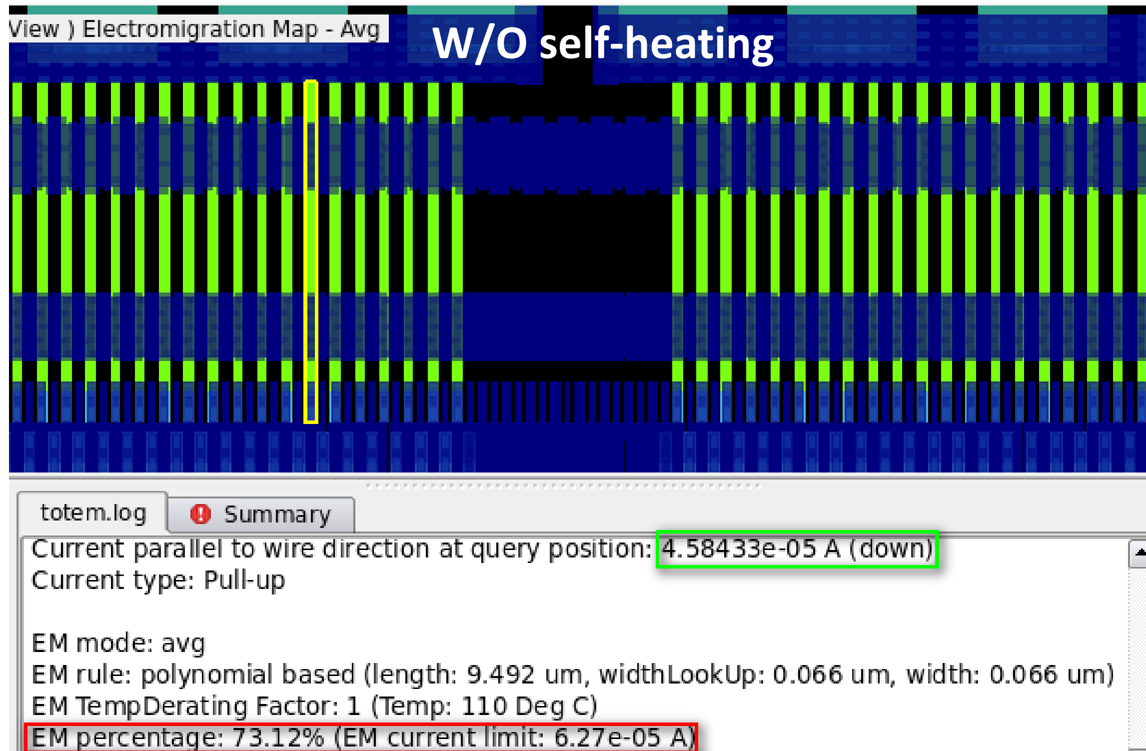
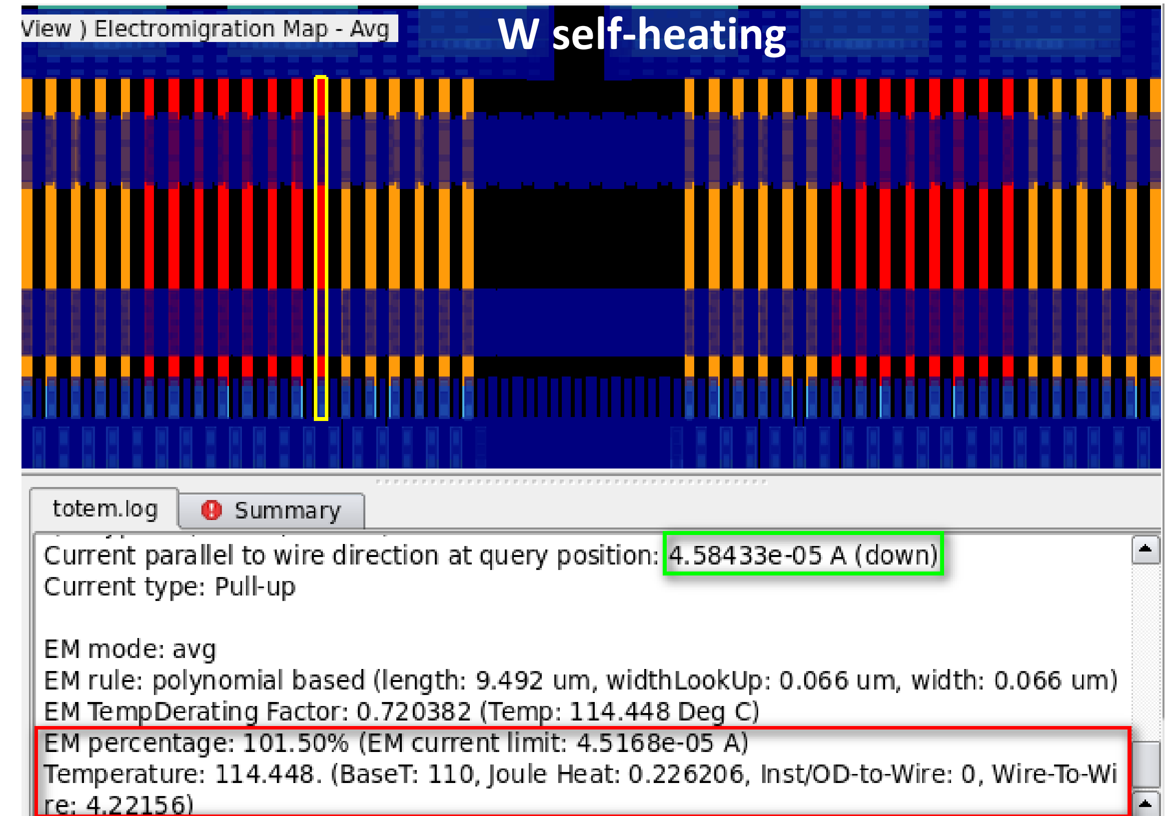
Thermal-Aware Statistical EM Result

- Self-heating degrade lifetime of interconnections significantly
- After considering the self-heating effect, potential EM risks can be detected





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Summary

- Quick power-critical window identification is essential for vcd-based IR analysis
- Power scaling analysis across PVT corners helps power calculation for PI signoff
- More PVT corner should be covered for PI analysis at advanced process
- RedHawk-SC showed 6X speedup compared to legacy multi-thread(DMP) computing
- Thermal-Aware Statistical EM is a must for advanced process

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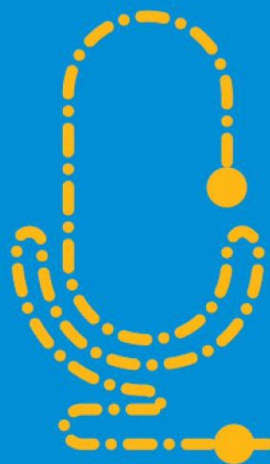
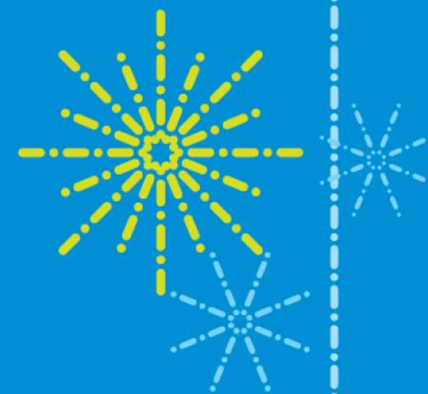
Thank you





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